

PHP/PHB45NQ15T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 8 November 2004

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Low thermal resistance
- Fast switching
- Low gate charge.

1.3 Applications

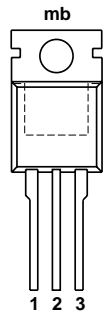
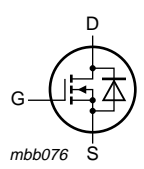
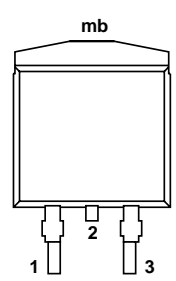
- DC-to-DC primary side switching
- AC-to-DC secondary side rectification.

1.4 Quick reference data

- $V_{DS} \leq 150 \text{ V}$
- $R_{DS(on)} \leq 42 \text{ m}\Omega$
- $I_D \leq 45.1 \text{ A}$
- $Q_{gd} = 10.3 \text{ nC (typ.)}$.

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate		
2	drain ^[1]		
3	source		
mb	mounting base; connected to drain		
			
		SOT78 (TO-220AB)	SOT404 (D²-PAK)

[1] It is not possible to make a connection to pin 2 of the SOT404 package.

3. Ordering information

Table 2: Ordering information

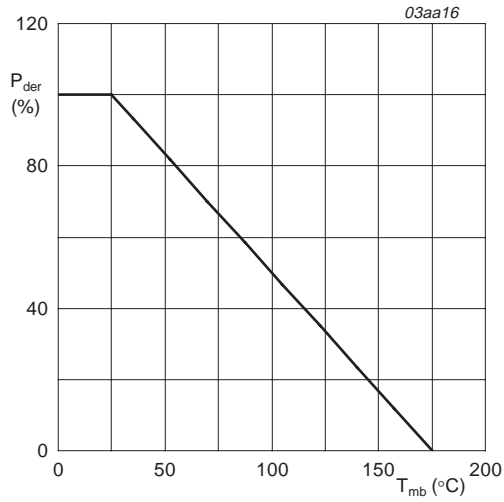
Type number	Package		Version
	Name	Description	
PHP45NQ15T	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 lead TO-220AB	SOT78
PHB45NQ15T	D ² -PAK	Plastic single-ended surface mounted package (D ² -PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 3: Limiting values

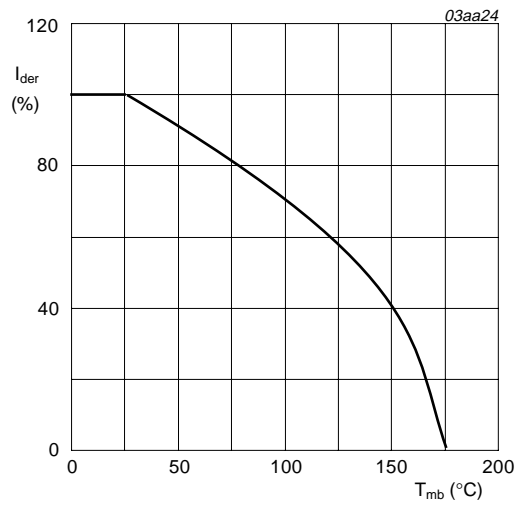
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage (DC)	25 °C ≤ T _j ≤ 175 °C	-	150	V
V _{DGR}	drain-gate voltage (DC)	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	150	V
V _{GS}	gate-source voltage (DC)		-	±20	V
I _D	drain current (DC)	T _{mb} = 25 °C; V _{GS} = 10 V; Figure 2 and 3	-	45.1	A
		T _{mb} = 100 °C; V _{GS} = 10 V; Figure 2	-	31.9	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3	-	90.2	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Figure 1	-	230	W
T _{stg}	storage temperature		-55	+175	°C
T _j	junction temperature		-55	+175	°C
Source-drain diode					
I _S	source (diode forward) current (DC)	T _{mb} = 25 °C	-	45.1	A
I _{SM}	peak source (diode forward) current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs	-	90.2	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I _D = 19.1 A; t _p = 0.1 ms; V _{DD} ≤ 150 V; R _{GS} = 50 Ω; V _{GS} = 10 V; starting at T _j = 25 °C	-	180	mJ



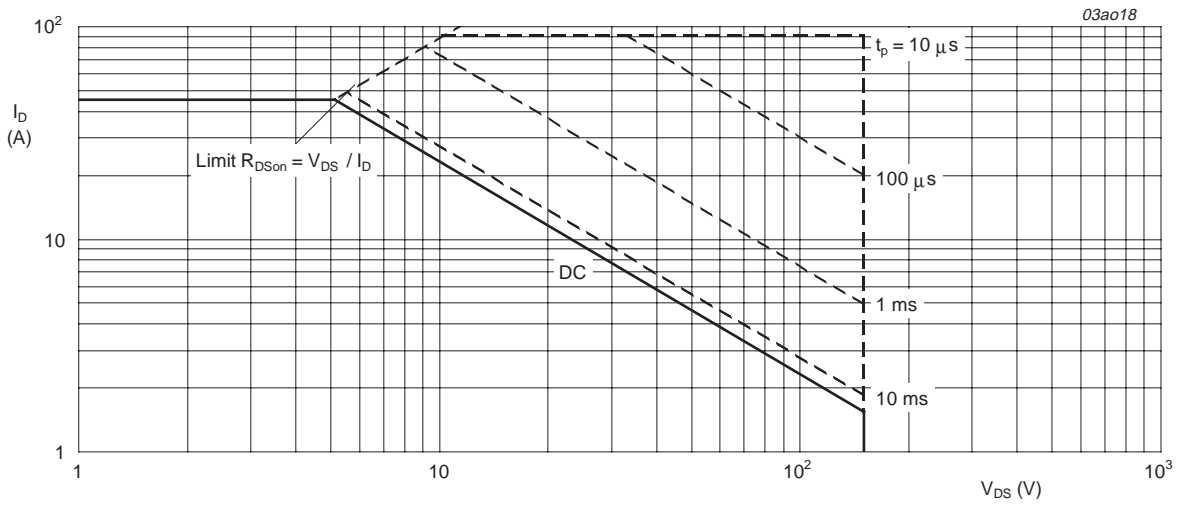
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.65	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in free air	-	60	-	K/W
	SOT404	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W

5.1 Transient thermal impedance

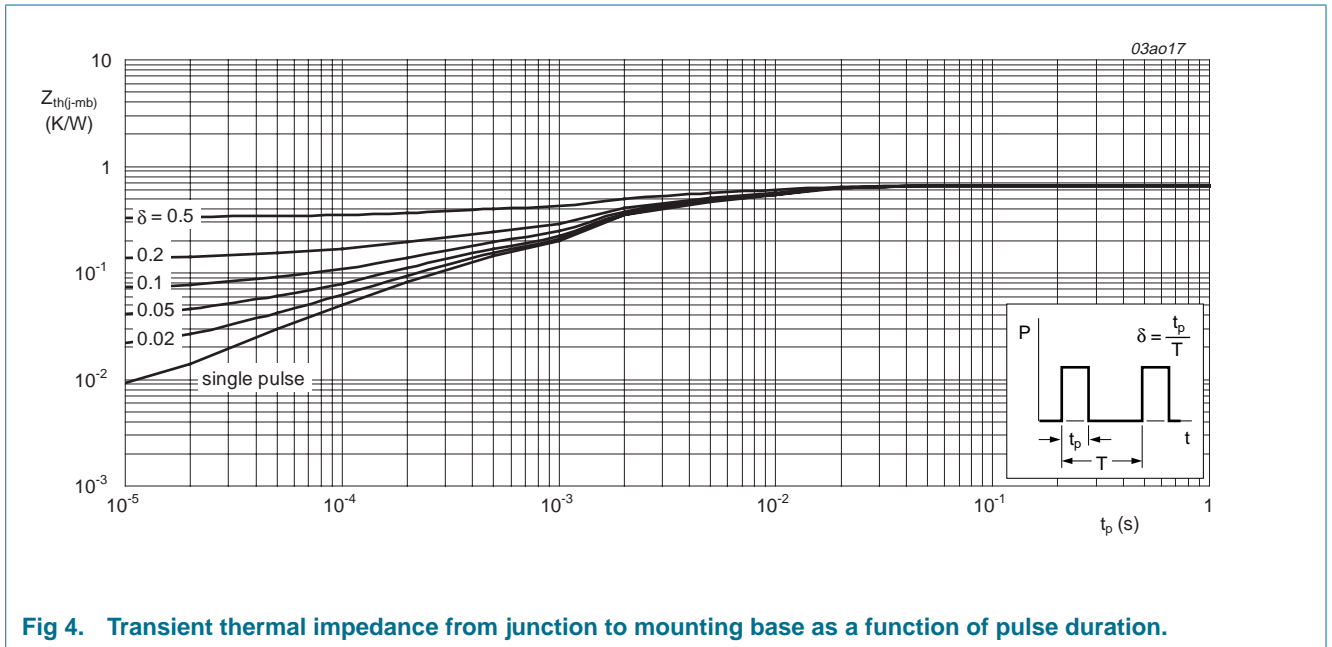
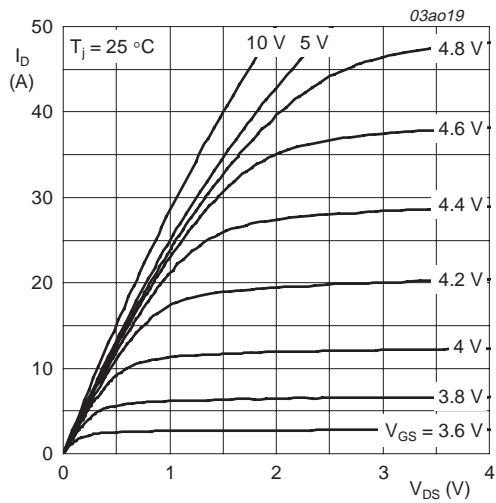


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

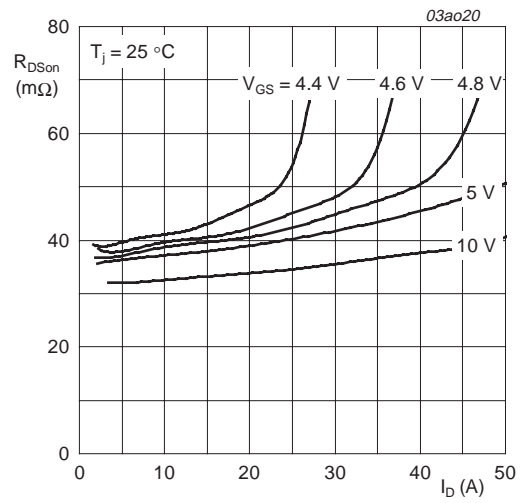
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V				
		T _j = 25 °C	150	-	-	V
		T _j = -55 °C	135	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10				
		T _j = 25 °C	2	3	4	V
		T _j = 175 °C	1	-	-	V
		T _j = -55 °C	-	-	4.4	V
I _{DSS}	drain-source leakage current	V _{DS} = 120 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	1	μA
		T _j = 175 °C	-	-	100	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 20 A; Figure 6 and 8				
		T _j = 25 °C	-	34	42	mΩ
		T _j = 175 °C	-	91.8	113.4	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 25 A; V _{DS} = 75 V; V _{GS} = 10 V; Figure 11	-	32	-	nC
Q _{gs}	gate-source charge		-	5.6	-	nC
Q _{gd}	gate-drain (Miller) charge		-	10.3	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 13	-	1770	-	pF
C _{oss}	output capacitance		-	290	-	pF
C _{rss}	reverse transfer capacitance		-	90	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 75 V; R _L = 3 Ω;	-	11.5	-	ns
t _r	rise time	V _{GS} = 10 V; R _G = 5.6 Ω	-	22	-	ns
t _{d(off)}	turn-off delay time		-	42	-	ns
t _f	fall time		-	31	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 12	-	0.88	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	115	-	ns
Q _r	recovered charge		-	360	-	nC



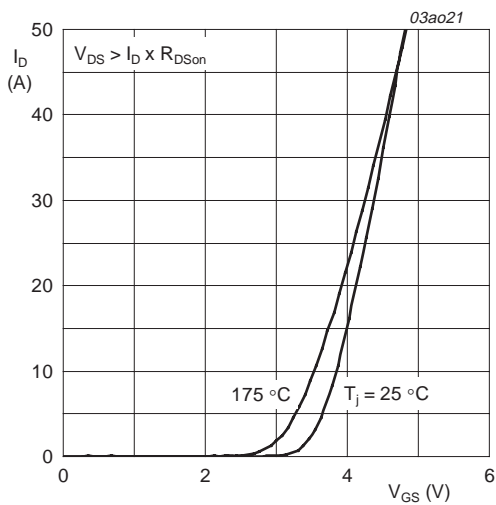
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



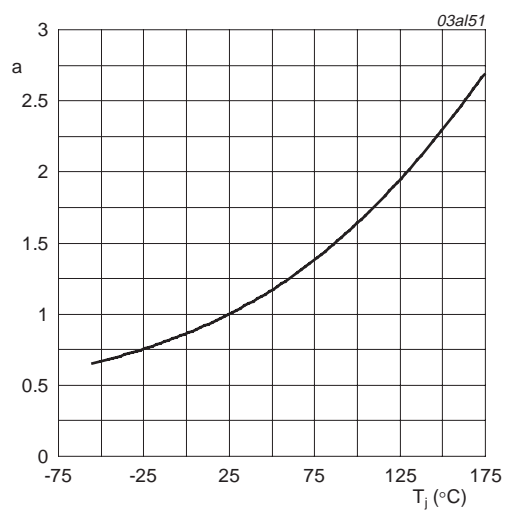
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



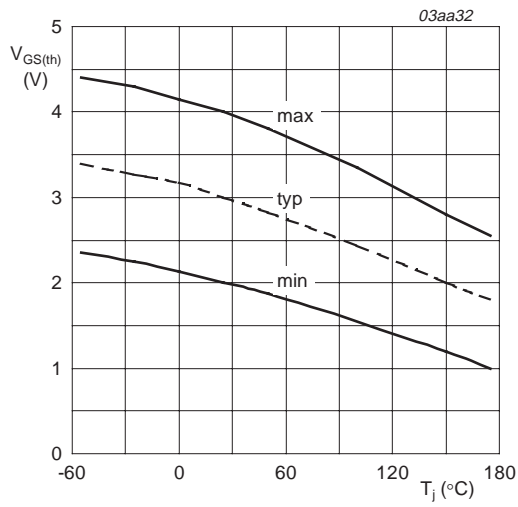
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



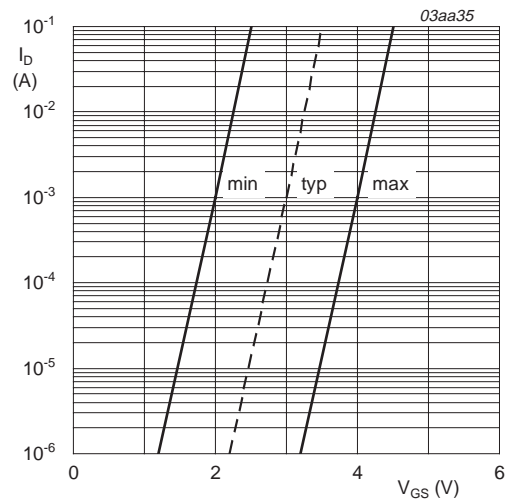
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



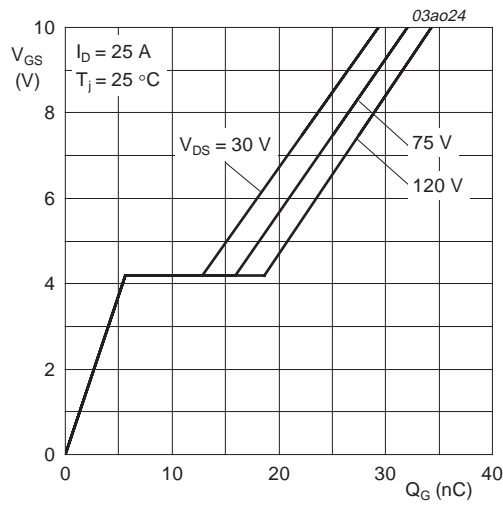
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



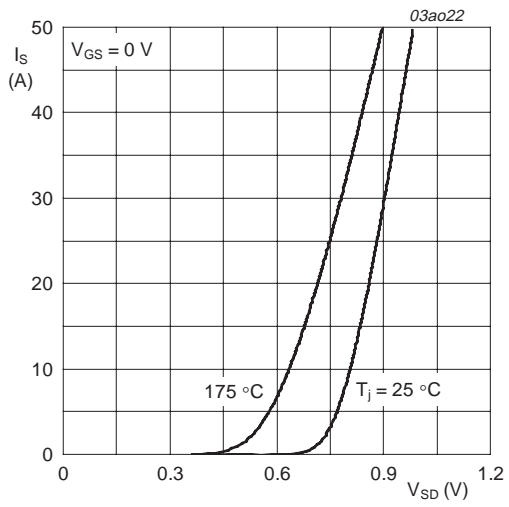
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



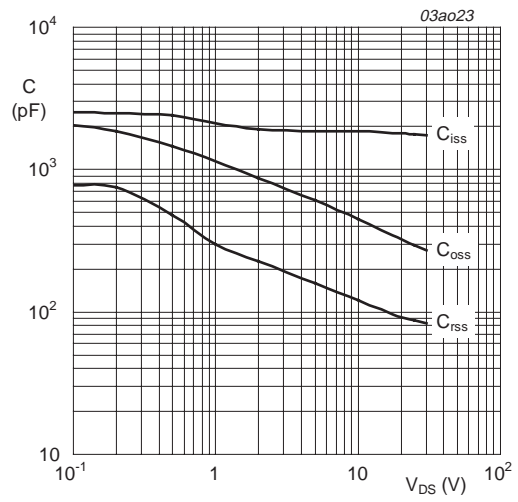
$I_D = 25 \text{ A}; V_{DS} = 30 \text{ V}, 75 \text{ V and } 120 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values.



$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

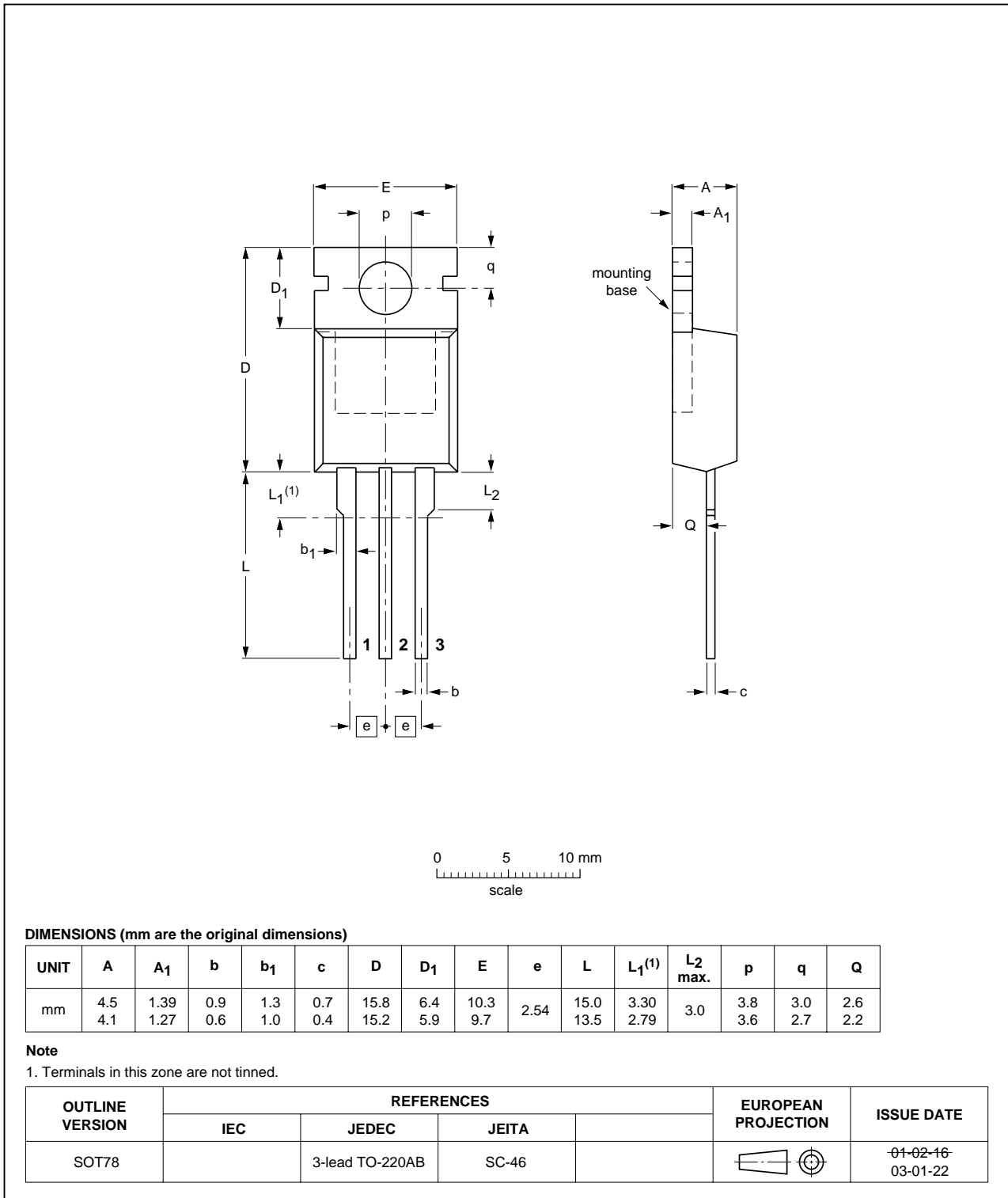


Fig 14. SOT78 (TO-220AB) package outline.

Plastic single-ended surface mounted package (D²-PAK); 3 leads (one lead cropped)

SOT404

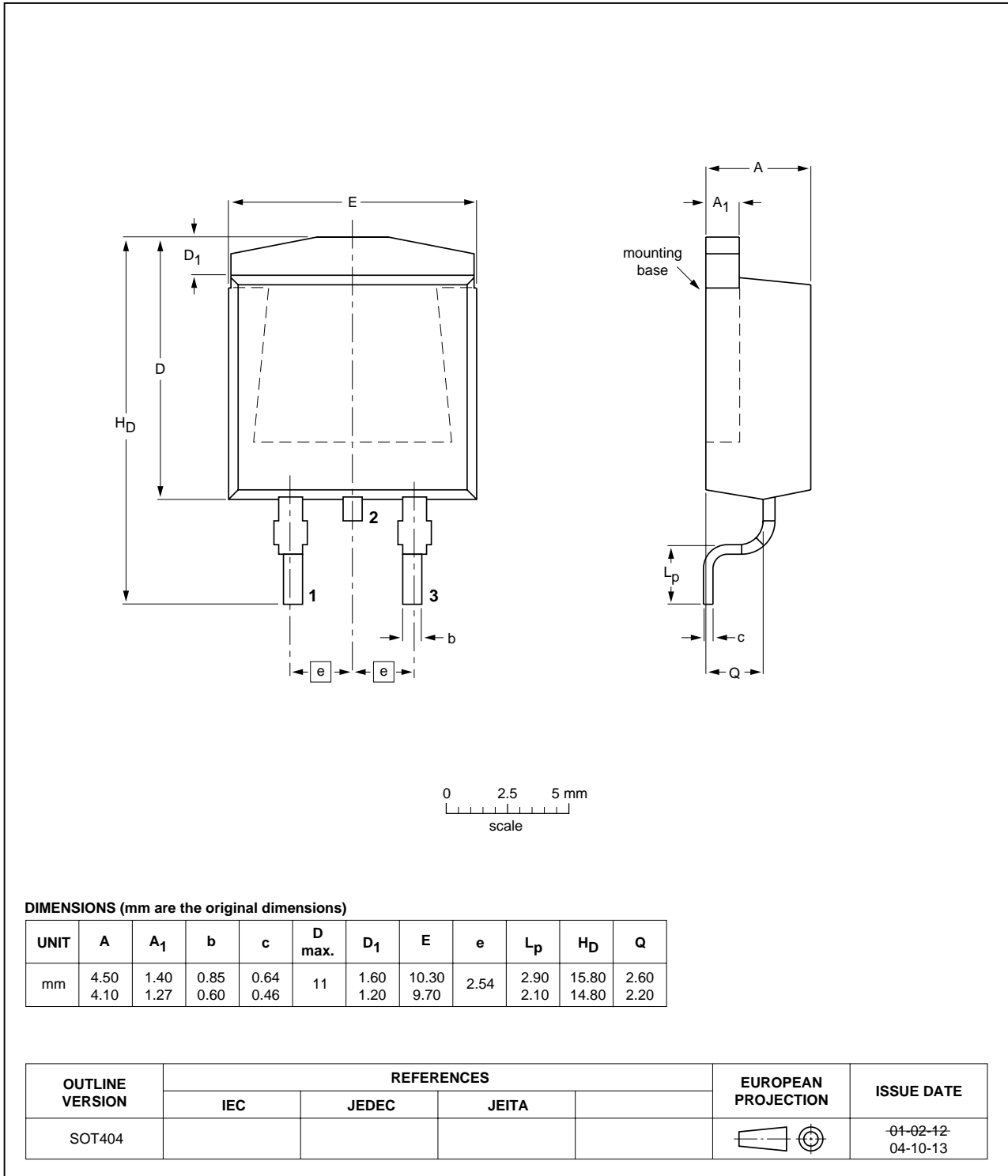


Fig 15. SOT404 (D²-PAK) package outline.



8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PHP_PHB45NQ15T_1	20041108	Product data sheet	-	9397 750 14012	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Date of release: 8 November 2004
Document number: 9397 750 14012

Published in The Netherlands