

64 K × 4 Static RAM with Separate IO

Features

- High speed
 - 15 ns
- CMOS for optimum speed/power
- Low active power
 - 860 mW
- Low standby power
 - 55 mW
- TTL-compatible inputs and outputs
- Automatic power down when deselected
- Available in Pb-free 28-pin Molded SOJ package

Functional Description

The CY7C192 is a high performance CMOS static RAM organized as 65,536 × 4 bits with separate IO. Easy memory expansion is provided by active LOW Chip Enable (\overline{CE}) and tri-state drivers. It has an automatic power down feature that reduces power consumption by 75% when deselected.

Writing to the device is accomplished when the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs are both LOW.

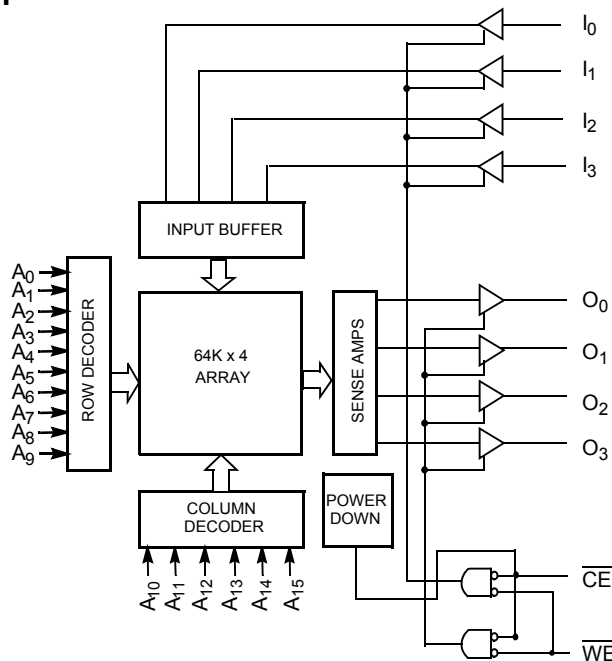
Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the Chip Enable (\overline{CE}) LOW while the Write Enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins appears on the four data output pins.

The output pins stay in high impedance state when Write Enable (\overline{WE}) is LOW or Chip Enable (\overline{CE}) is HIGH.

A die coat ensures alpha immunity.

Logic Block Diagram

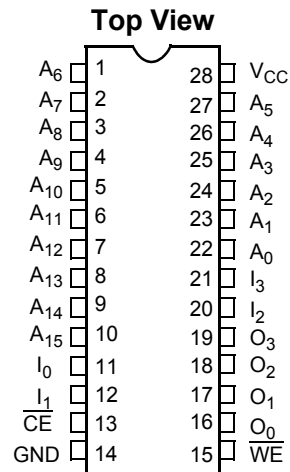


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Pin Configurations

Figure 1. 28-pin Molded SOJ pinout



Selection Guide

| Description | -15 | Unit |
|------------------------------|-----|------|
| Maximum Access Time | 15 | ns |
| Maximum Operating Current | 145 | mA |
| Maximum CMOS Standby Current | 10 | mA |

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| | |
|--|-----------------------------------|
| Storage Temperature | -65 °C to +150 °C |
| Ambient Temperature with Power Applied | -55 °C to +125 °C |
| Supply Voltage to Ground Potential | -0.5 V to +7.0 V |
| DC Voltage Applied to Outputs in High Z State ^[1] | -0.5 V to V _{CC} + 0.5 V |

| | |
|---|-----------------------------------|
| DC Input Voltage ^[1] | -0.5 V to V _{CC} + 0.5 V |
| Output Current into Outputs (LOW) | 20 mA |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | > 900 V |
| Latch-Up Current | > 200 mA |

Operating Range

| Range | Ambient Temperature ^[2] | V _{CC} |
|------------|------------------------------------|-----------------|
| Commercial | 0 °C to +70 °C | 5 V ± 10% |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | -15 | | Unit |
|------------------|--|---|------|-----------------------|------|
| | | | Min | Max | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min, I _{OH} = -4.0 mA | 2.4 | - | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min, I _{OL} = 8.0 mA | - | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -5 | +5 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -5 | +5 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | - | 145 | mA |
| I _{SB1} | Automatic \overline{CE} Power Down Current – TTL Inputs | Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | - | 30 | mA |
| I _{SB2} | Automatic \overline{CE} Power Down Current – CMOS Inputs | Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} - 0.3 V or V _{IN} ≤ 0.3 V, f = 0 | - | 10 | mA |

Capacitance

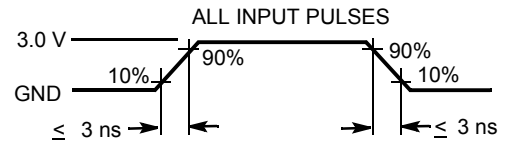
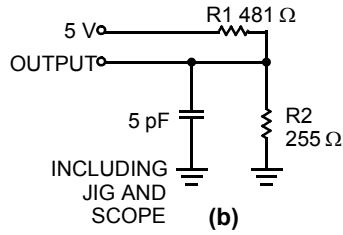
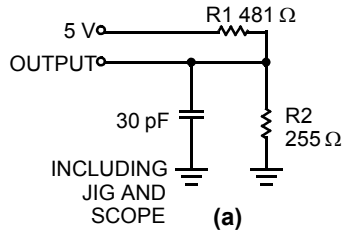
| Parameter | Description | Test Conditions | Max | Unit |
|---------------------------------|--------------------|--|-----|------|
| C _{IN} ^[3] | Input Capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V | 8 | pF |
| C _{OUT} ^[3] | Output Capacitance | | 10 | pF |

Notes

1. Minimum voltage is equal to -2.0 V for pulse durations of less than 20 ns.
2. T_A is the case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 $167\ \Omega$
 OUTPUT $1.73\ \text{V}$

Switching Characteristics

Over the Operating Range

| Parameter ^[4] | Description | -15 | | Unit |
|-----------------------------------|--|-----|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read Cycle Time | 15 | – | ns |
| t_{AA} | Address to Data Valid | – | 15 | ns |
| t_{OHA} | Output Hold from Address Change | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | – | 15 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[5] | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[5, 6] | – | 7 | ns |
| t_{PU} | \overline{CE} LOW to Power Up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to Power Down | – | 15 | ns |
| Write Cycle ^[7] | | | | |
| t_{WC} | Write Cycle Time | 15 | – | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 10 | – | ns |
| t_{AW} | Address Setup to Write End | 10 | – | ns |
| t_{HA} | Address Hold from Write End | 0 | – | ns |
| t_{SA} | Address Setup to Write Start | 0 | – | ns |
| t_{PWE} | \overline{WE} Pulse Width | 9 | – | ns |
| t_{SD} | Data Setup to Write End | 9 | – | ns |
| t_{HD} | Data Hold from Write End | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[5] | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[5, 6] | – | 7 | ns |

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of [Figure 2](#). Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1 [8, 9]

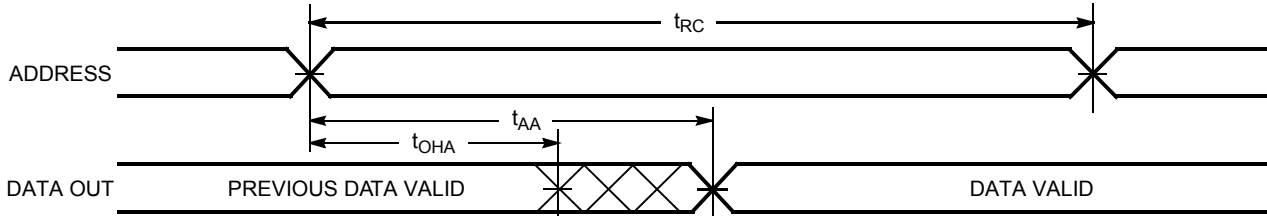


Figure 4. Read Cycle No. 2 [8, 10]

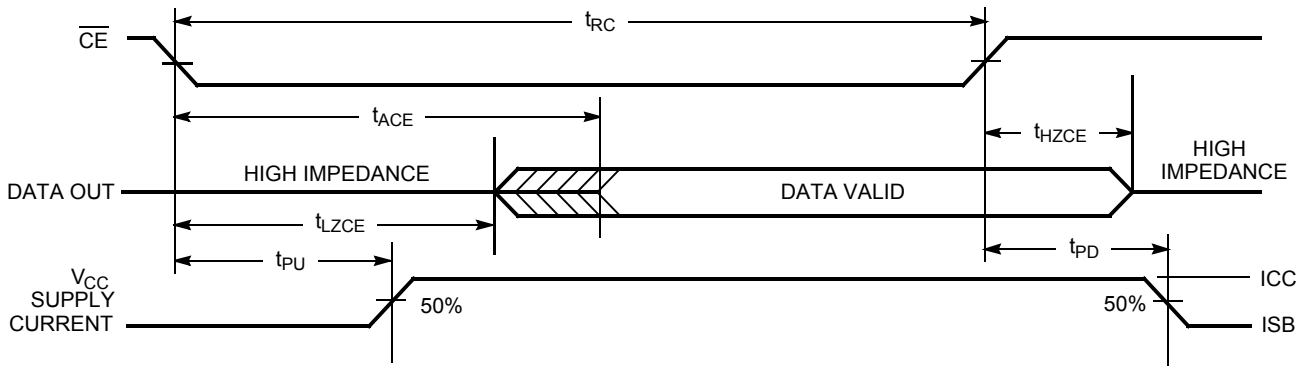
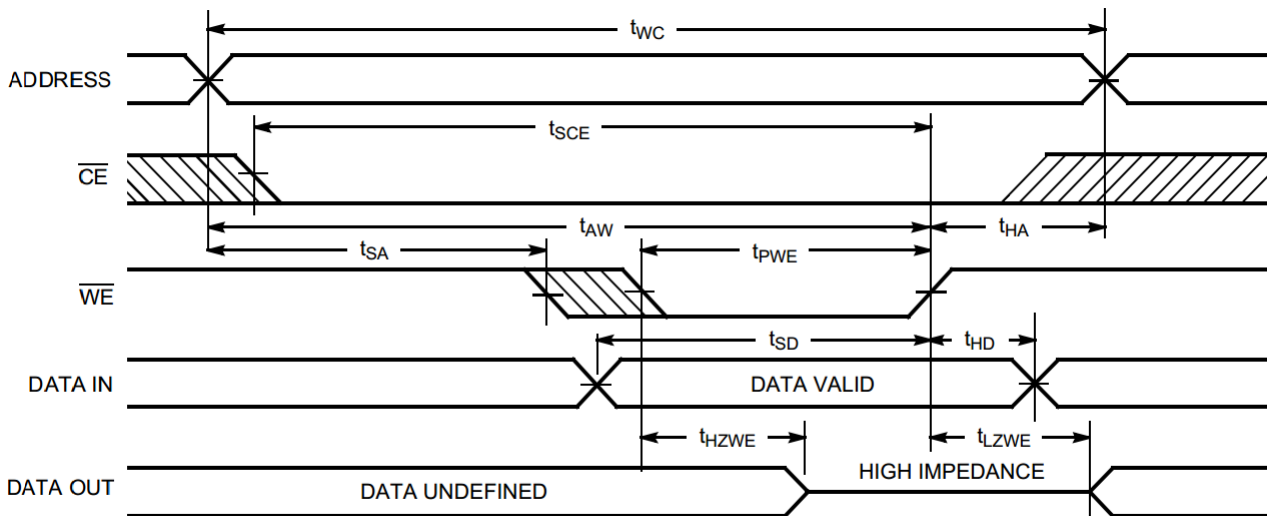


Figure 5. Write Cycle No. 1 (\overline{WE} Controlled) [11]

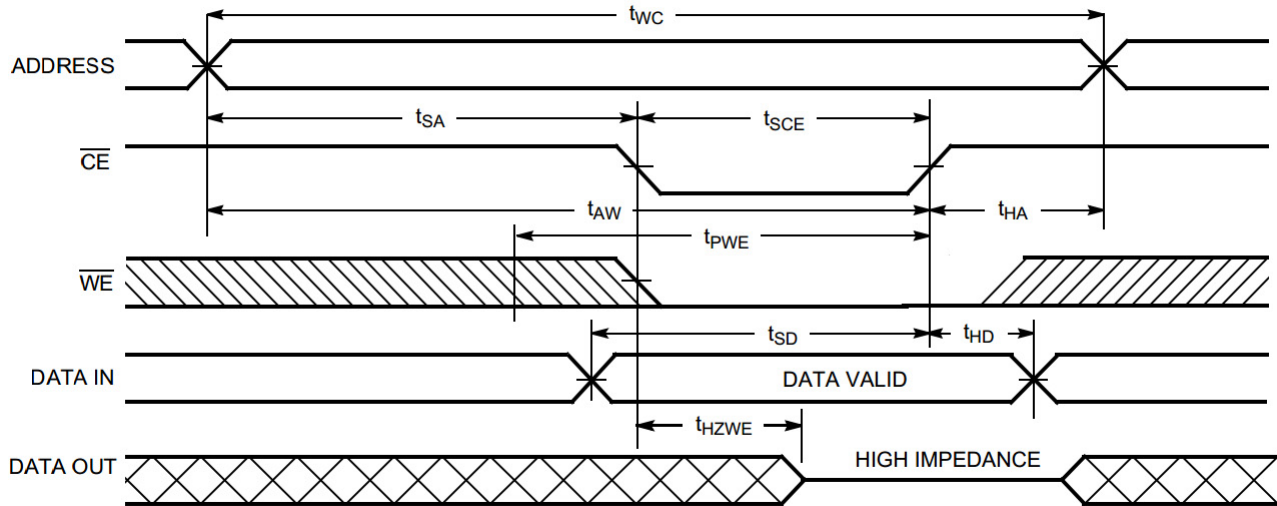


Notes

8. \overline{WE} is HIGH for read cycle.
9. Device is continuously selected, $\overline{CE} = V_{IL}$.
10. Address valid prior to or coincident with \overline{CE} transition LOW.
11. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)

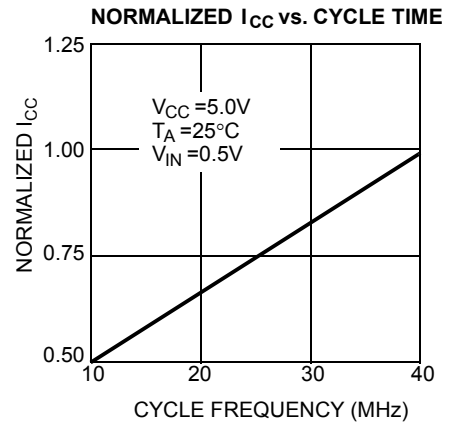
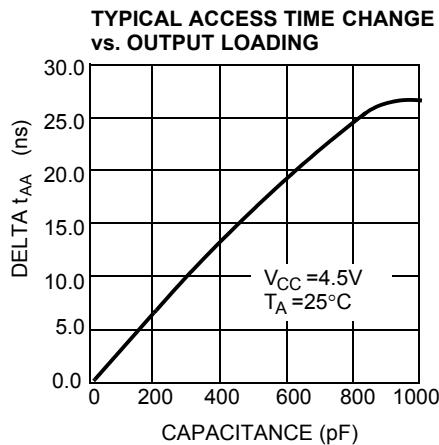
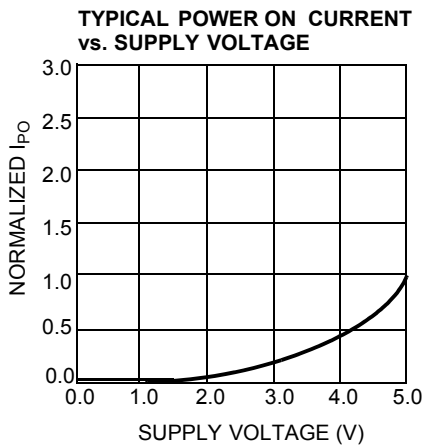
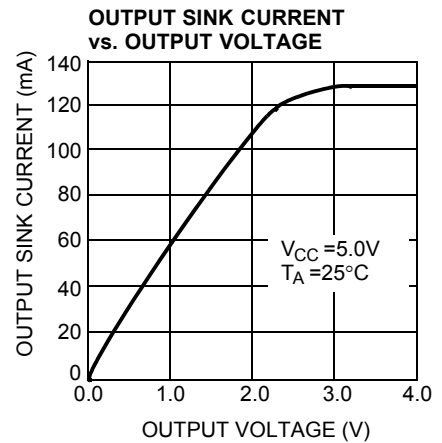
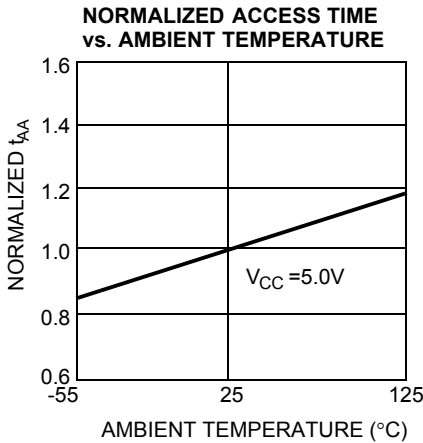
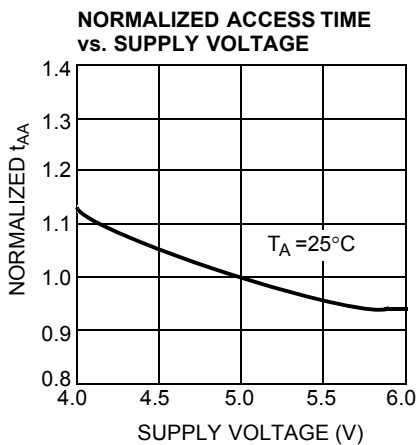
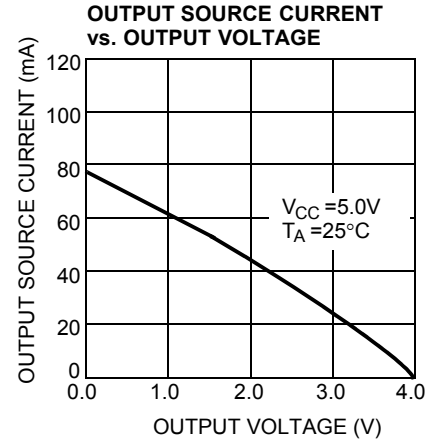
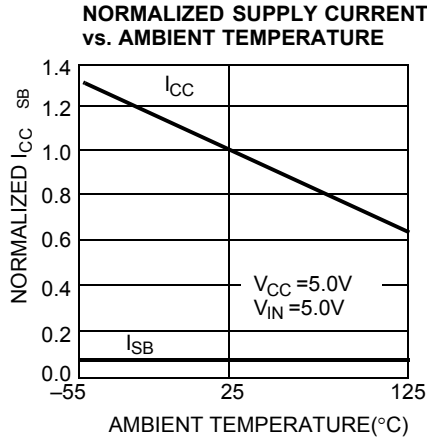
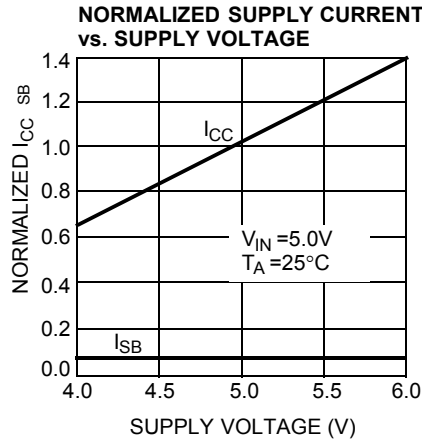
Figure 6. Write Cycle No. 2 (\overline{CE} Controlled) [12, 13]



Notes

12. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.

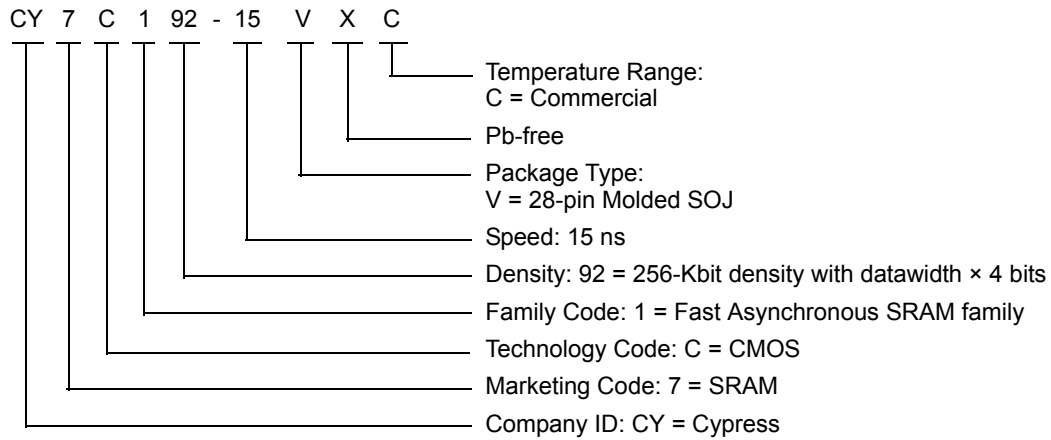
Typical DC and AC Characteristics



Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------|-----------------|-----------------------------|-----------------|
| 15 | CY7C192-15VXC | 51-85031 | 28-pin Molded SOJ (Pb-free) | Commercial |

Ordering Code Definitions

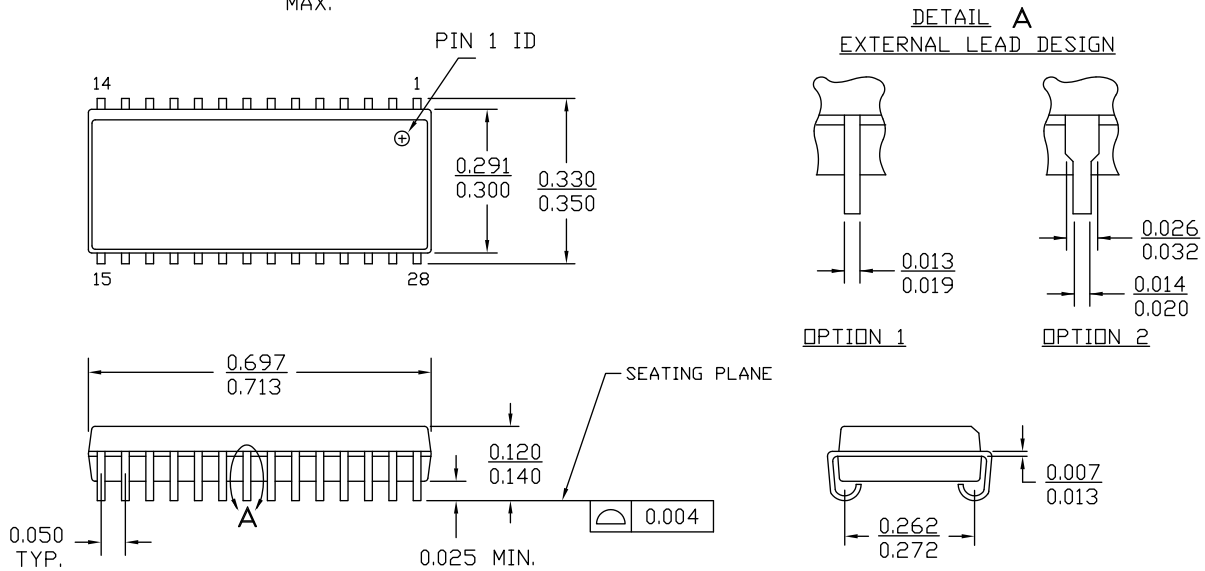


Package Diagram

Figure 7. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.
MAX.



51-85031 *E

Acronyms

| Acronym | Description |
|---------|---|
| CE | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| SOJ | Small Outline J-lead |
| SRAM | Static Random Access Memory |
| TTL | Transistor-Transistor Logic |
| WE | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celcius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mW | milliwatt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C192, 64 K × 4 Static RAM with Separate IO | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-05047 | | | | |
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 107149 | 09/10/01 | SZV | Change Spec number from: 38-00076 to 38-05047 |
| *A | 359716 | See ECN | AJU | Changed Static Discharge Voltage limit in the Maximum Ratings section (page 2) from 2001V to 900V Removed references to CY7C191 |
| *B | 419549 | See ECN | AJU | Added Pb-free parts to the Ordering Information table and replaced the Package Name column with Package Diagram |
| *C | 492500 | See ECN | NXR | Removed 20 ns and 25 ns speed bins Changed the Low active power from 220 mW to 55 mW Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Removed 28-Lead (300-Mil) PDIP package from product offering Updated Ordering Information table |
| *D | 2104606 | See ECN | VKN/AESA | Removed 12 ns speed bin |
| *E | 2956606 | 06/18/2010 | KAO | Removed inactive part from Ordering Information Updated Package Diagram . Added Sales, Solutions, and Legal Information . |
| *F | 3105329 | 12/09/2010 | AJU | Added Ordering Code Definitions . |
| *G | 3217855 | 04/06/2011 | PRAS | Added Acronyms and Units of Measure . Updated in new template. |
| *H | 3271782 | 06/01/2011 | PRAS | Updated Features . |
| *I | 3974483 | 04/19/2013 | MEMJ | Updated Switching Waveforms (Updated Figure 5 , Figure 6). Updated Package Diagram : spec 51-85031 – Changed revision from *D to *E. Completing Sunset Review. |

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