AOT502

Clamped N-Channel MOSFET

ALPHA & OMEGA SEMICONDUCTOR

General Description

AOT502 uses an optimally designed temperature compensated gate-drain zener clamp. Under overvoltage conditions, the clamp activates and turns on the MOSFET, safely dissipating the energy in the MOSFET.
The built in resistor guarantees proper clamp operation under all circuit conditions, and the MOSFET never goes into avalanche breakdown. Advanced trench technology provides excellent low Rdson, gate charge and body diode characteristics, making this device ideal for motor and inductive load control applications.

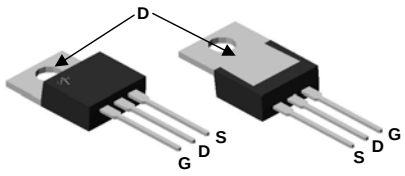
Product Summary

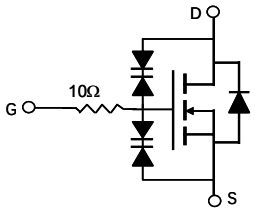
V_{DS}	Clamped
I_D (at V_{GS}=10V)	60A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 11.5mΩ

100% UIS Tested
100% R_g Tested

RoHS Compliant

TO220
Top View Bottom View





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	Clamped	V
Gate-Source Voltage		V_{GS}	Clamped	V
Continuous Drain Current	T_C=25°C	I_D	60	A
	T_C=100°C		41	
Pulsed Drain Current [C]		I_{DM}	137	
Continuous Drain Current	T_A=25°C	I_{DSM}	9	A
	T_A=70°C		7	
Avalanche Current [C]		I_{AS}, I_{AR}	28.5	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	41	mJ
Power Dissipation [B]	T_C=25°C	P_D	79	W
	T_C=100°C		39	
Power Dissipation [A]	T_A=25°C	P_{DSM}	1.9	W
	T_A=70°C		1.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	13	15.6	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		54	65	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.6	1.9	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
$BV_{DSS(z)}$	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	33			V
BV_{CLAMP}	Drain-Source Clamping Voltage	I_D=1A, V_{GS}=0V	36		44	V
$I_{DSS(z)}$	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			20	µA
BV_{GSS}	Gate-Source Voltage	V_{DS}=0V, I_D=250µA	20			V
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±10V			10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	1.6	2.1	2.7	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	137			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=30A		9.3	11.5	mΩ
		T_J=125°C		15.4	18.5	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=30A		55		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.73	1	V
I_S	Maximum Body-Diode Continuous Current				75	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	960	1205	1450	pF
C_{oss}	Output Capacitance		185	266	345	pF
C_{rss}	Reverse Transfer Capacitance		65	109	155	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	10	20	30.0	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=30A	18.5	23.4	28	nC
Q_{gs}	Gate Source Charge		2.7	3.4	4	nC
Q_{gd}	Gate Drain Charge		4	7	10	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.5Ω, R_{GEN}=3Ω		13.5		ns
t_r	Turn-On Rise Time			17.5		ns
$t_{D(off)}$	Turn-Off DelayTime			63		ns
t_f	Turn-Off Fall Time			27		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=30A, dI/dt=750A/µs	14	17.5	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=30A, dI/dt=750A/µs	53.5	67	80	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

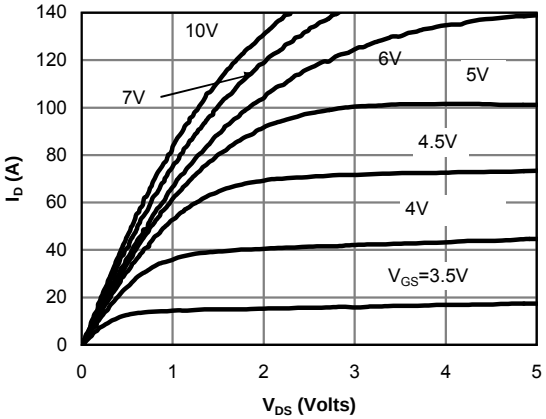


Fig 1: On-Region Characteristics (Note E)

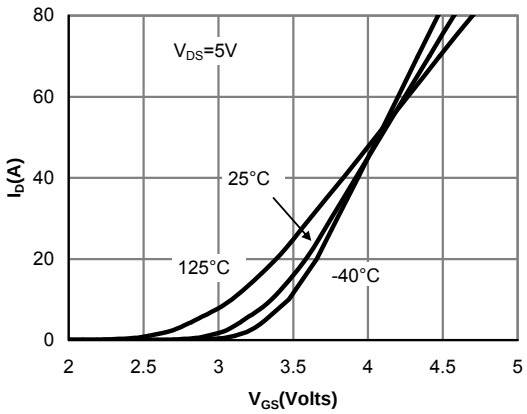


Figure 2: Transfer Characteristics (Note E)

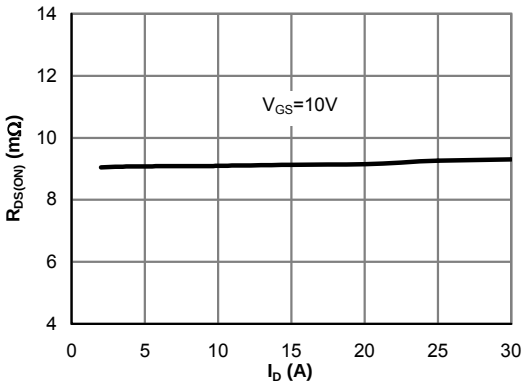


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

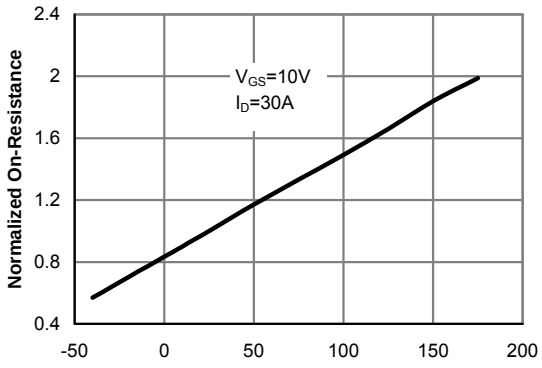


Figure 4: On-Resistance vs. Junction Temperature (Note E)

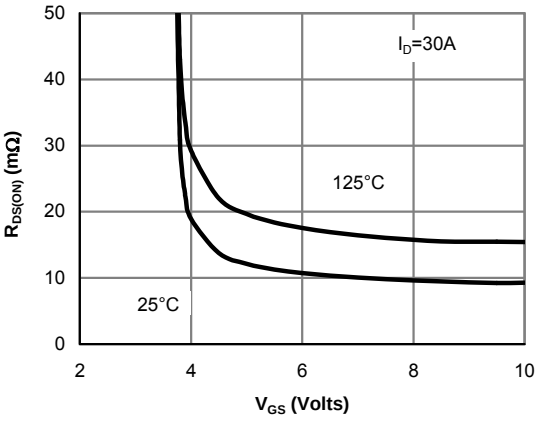


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

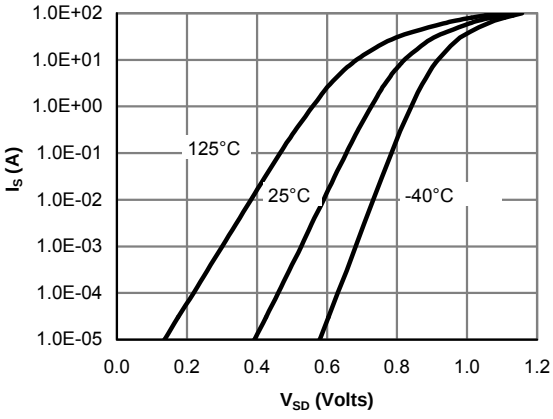


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

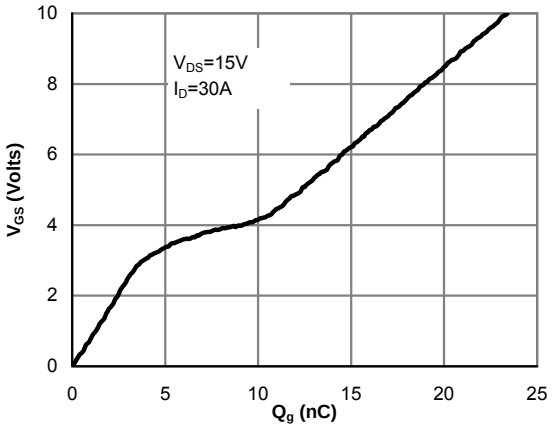


Figure 7: Gate-Charge Characteristics

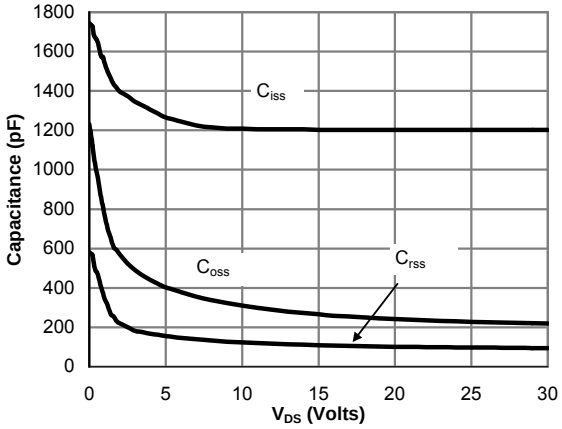


Figure 8: Capacitance Characteristics

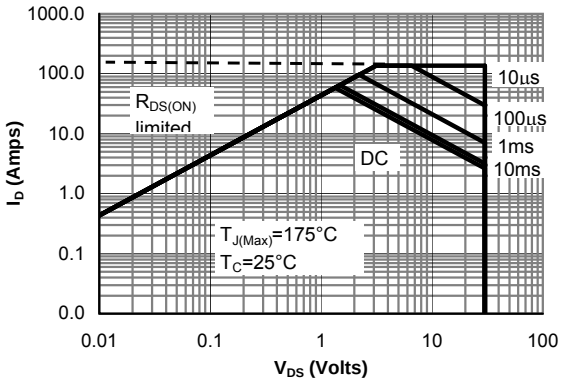


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

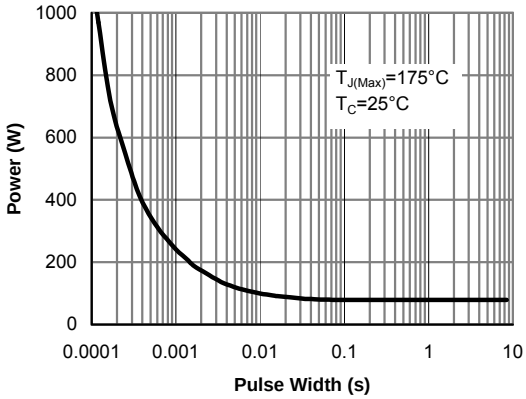


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

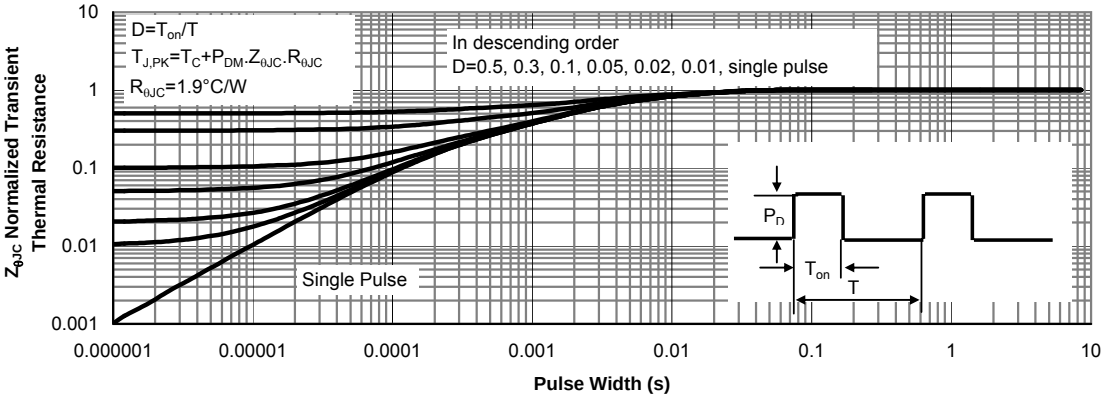


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

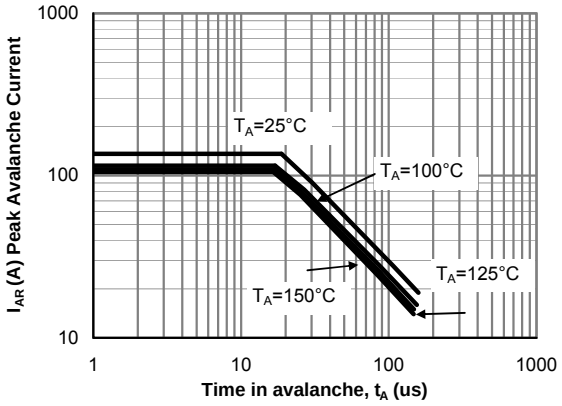


Figure 12: Single Pulse Avalanche capability (Note C)

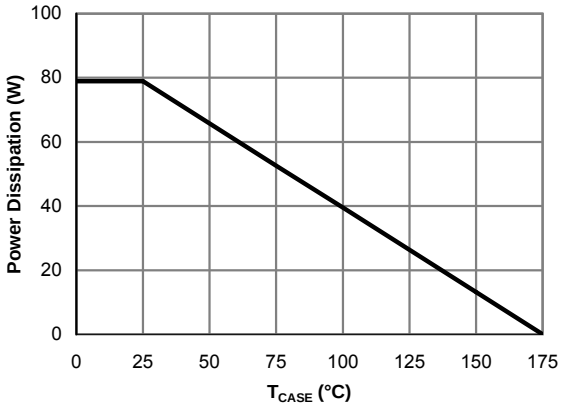


Figure 13: Power De-rating (Note F)

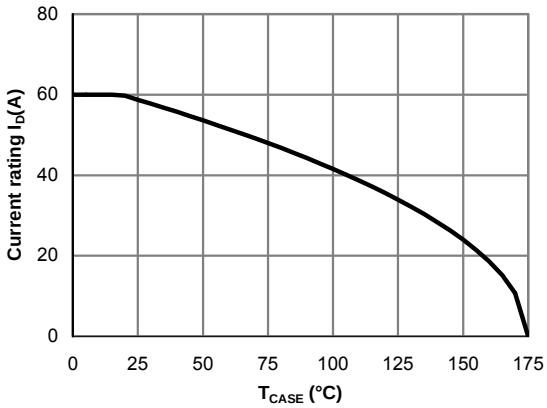


Figure 14: Current De-rating (Note F)

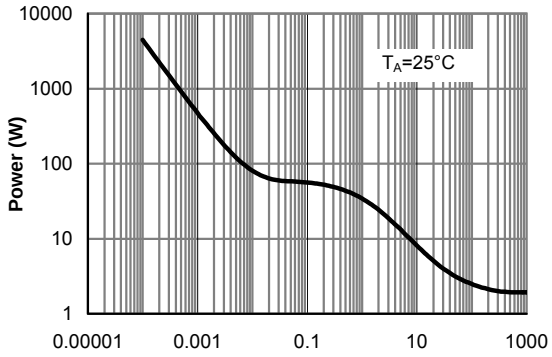


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

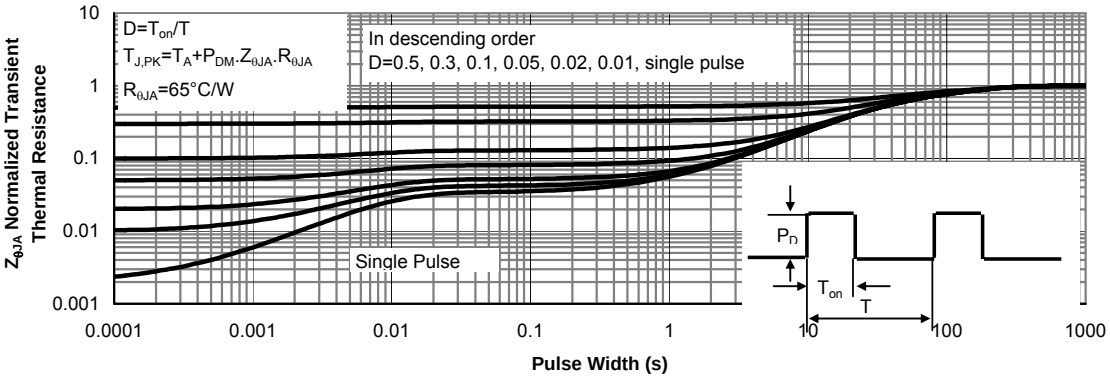
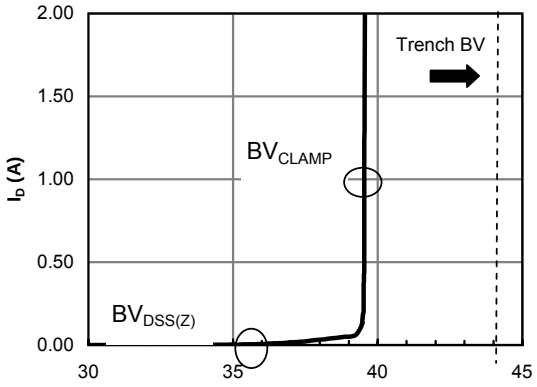


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL PROTECTION CHARACTERISTICS



V_{DS} (Volts)
Fig 15: BV_{CLAMP} Characteristic

This device uses built-in Gate to Source and Gate to Drain zener protection. While the Gate-Source zener protects against excessive V_{GS} conditions, the Gate to Drain protection, clamps the V_{DS} well below the device breakdown, preventing an avalanche condition within the MOSFET as a result of voltage over-shoot at the Drain electrode.
It is designed to breakdown well before the device breakdown. During such an event, current flows through the zener clamp, which is situated internally between the Gate to Drain. This current flows at $BV_{DSS(Z)}$, building up the V_{GS} internal to the device. When the current level through the zener reaches approximately 300mA, the V_{GS} is approximately equal to $V_{GS(PLATEAU)}$, allowing significant channel conduction and thus clamping the Drain to Source voltage. The V_{GS} needed to turn the device on is controlled with an internally lumped gate resistor R approximately equal to 10Ω.

$$V_{GS(PLATEAU)} = 10\Omega \times 300mA = 3V$$

It can also be said that the VDS during clamping is equal to:

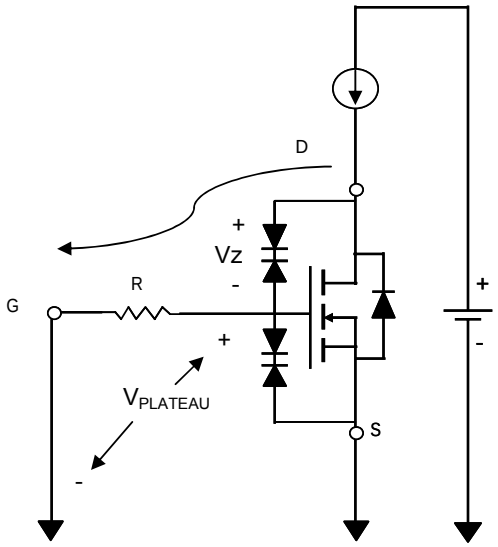
$$BV_{DSS} = BV_{CLAMP} + V_{GS(PLATEAU)}$$

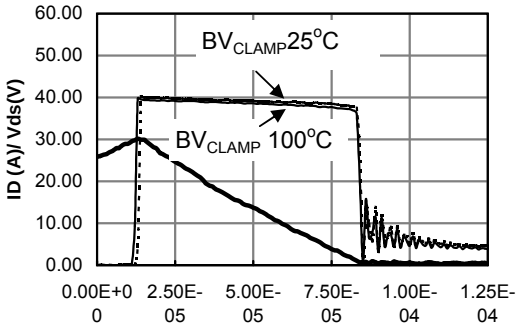
Additional power loss associated with the protection circuitry can be considered negligible when compare to the conduction losses of the MOSFET itself;

EX:

PL=30μAmax x 16V=0.48mW (Zener leakage loss)

$PL(rds)=10^2A \times 6m\Omega=300mW$ (MOSFET loss)

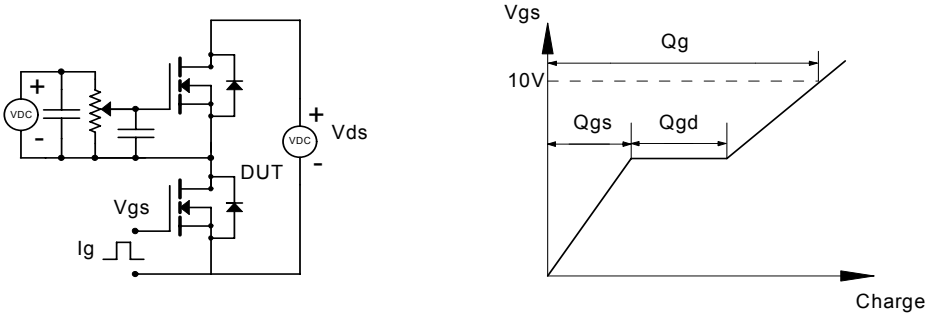




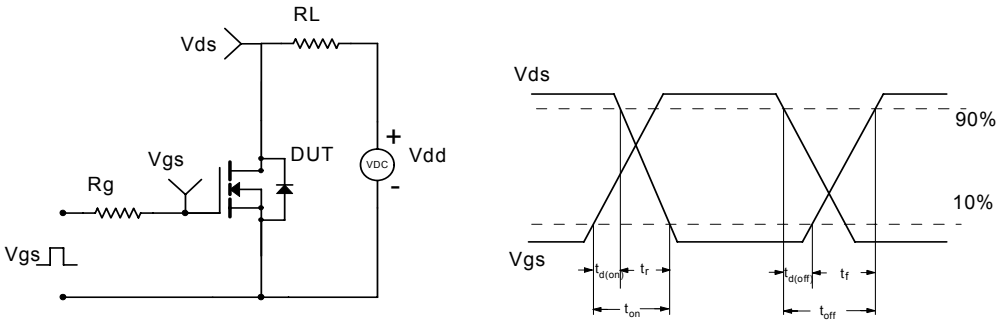
Time in Avalanche (Seconds)
Fig 16: Unclamped Inductive Switching

Fig16: The built-in Gate to Drain clamp prevents the device from going into Avalanche by setting the clamp voltage well below the actual breakdown of the device. When the Drain to Gate voltage approaches the BV clamp, the internal Gate to Source voltage is charged up and channel conduction occurs, sinking the current safely through the device. The BV_{CLAMP} is virtually temperature independent, providing even greater protection during normal operation.

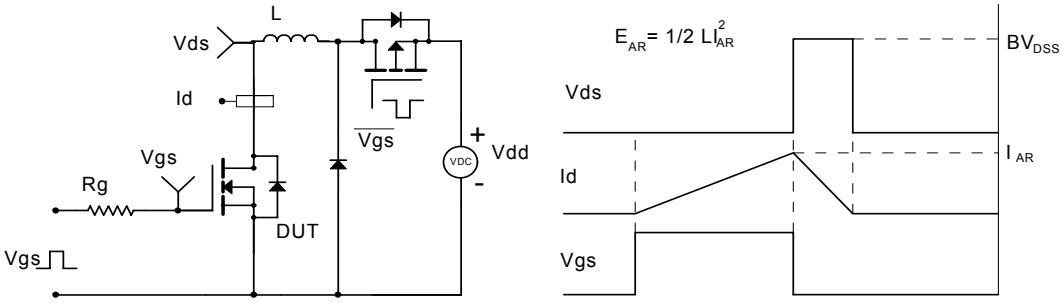
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms