ESD9101

Product Preview

ESD Protection Diode

Low Capacitance ESD Protection Diodes for High Speed Data Lines

The ESD9101 is designed to protect a single high speed data line from ESD. Ultra−low capacitance and low ESD clamping voltage via SCR technology make this device an ideal solution for protecting voltage sensitive high speed data lines. The SOD−923 mico−package allows for easy PCB layout and the ability to be placed in space constrained applications where board area comes at a premium.

Features

- Low Capacitance (0.5 pF Max, I/O to GND)
- Protection for the Following Standards: IEC 61000−4−2 (Level 4) & ISO 10605
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.0/3.1
- HDMI 1.3/1.4/2.0
- DisplayPort
- GPS Antenna

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact IEC 61000−4−2 Air ISO 10605 150 pF/2 kΩ ISO 10605 330 pF/2 kΩ ISO 10605 330 pF/330 Ω	ESD	±25 ±25 ±30 ±30 ±20	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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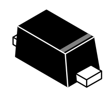
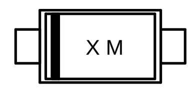
MARKING DIAGRAM

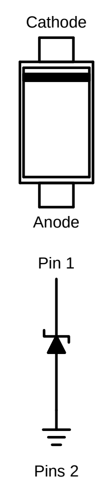


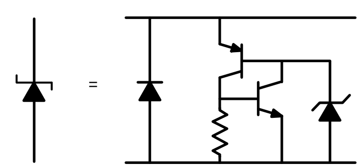
SOD−923
CASE 514AB



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATIONS AND SCHEMATICS





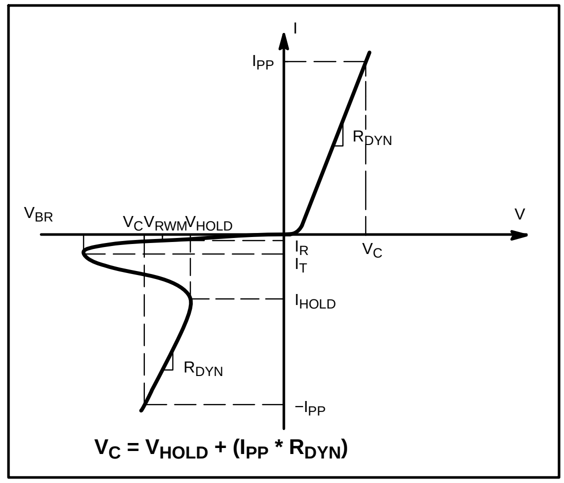
ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.3	7.0	8.0	V
Reverse Leakage Current	I_R	V_{RWM} = 5.0 V, I/O Pin to GND			1.0	μA
Holding Reverse Voltage	V_{HOLD}	I/O Pin to GND		2.2		V
Holding Reverse Current	I_{HOLD}	I/O Pin to GND	65	97		mA
Clamping Voltage	V_C	IEC61000−4−2, ±8 KV Contact	See Figures 1 and 2			V
Clamping Voltage TLP	V_C	I_{PP} = 8 A I_{PP} = −8 A I_{PP} = 16 A I_{PP} = −16 A		5.0 −4.0 7.0 −7.0		V
Dynamic Resistance	R_{DYN}	I/O Pin to GND GND to I/O Pin		0.30 0.38		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND V_R = 0 V, f = 2.5 GHz between I/O Pins and GND V_R = 0 V, f = 5.0 GHz between I/O Pins and GND		0.36 0.36 0.36	0.50 0.45 0.45	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

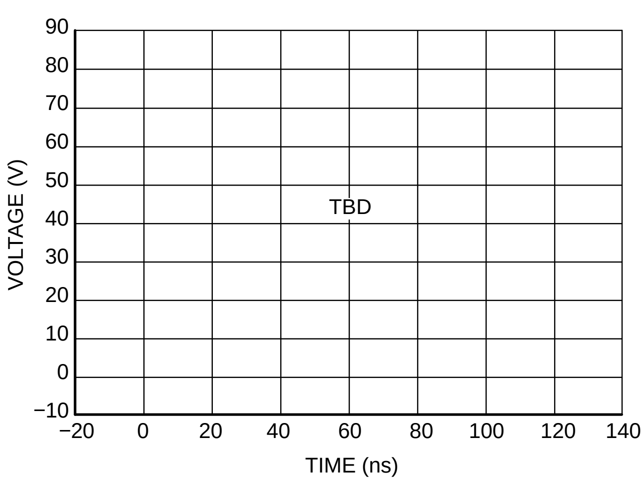


Figure 1. IEC61000−4−2 +8 kV Contact ESD Clamping Voltage

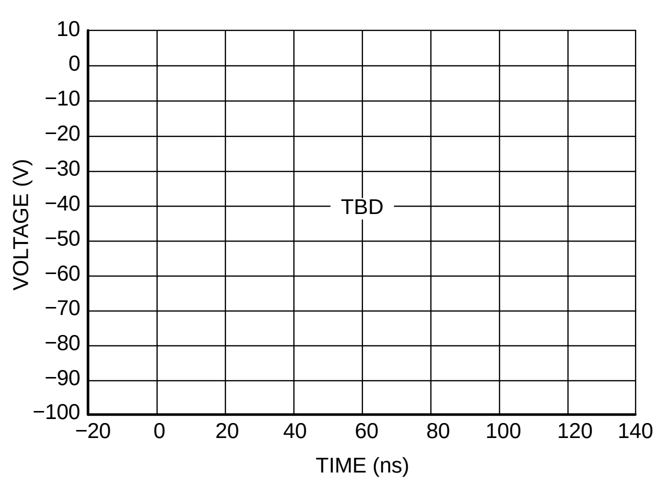


Figure 2. IEC61000−4−2 −8 kV Contact Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

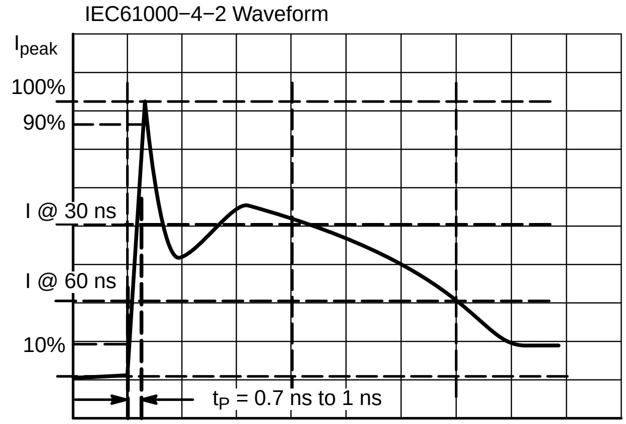


Figure 3. IEC61000−4−2 Spec

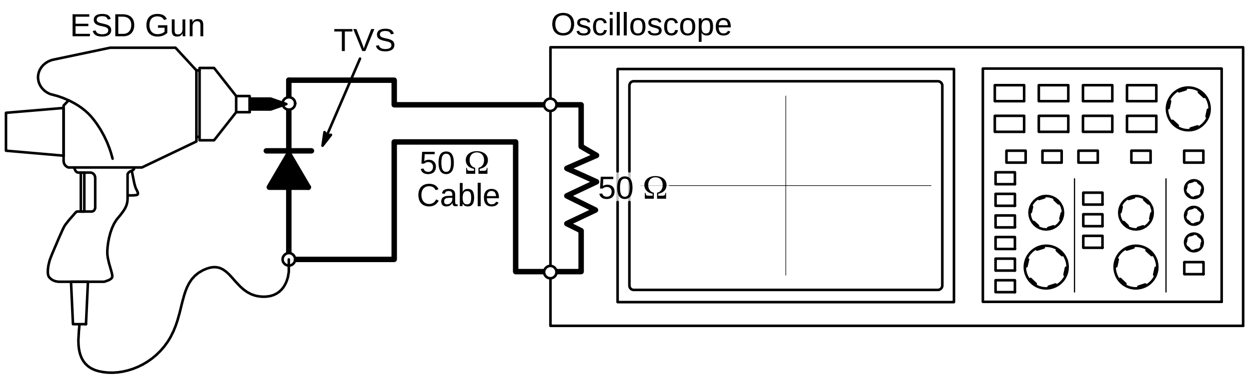


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D − Characterization of ESD Clamping Performance.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

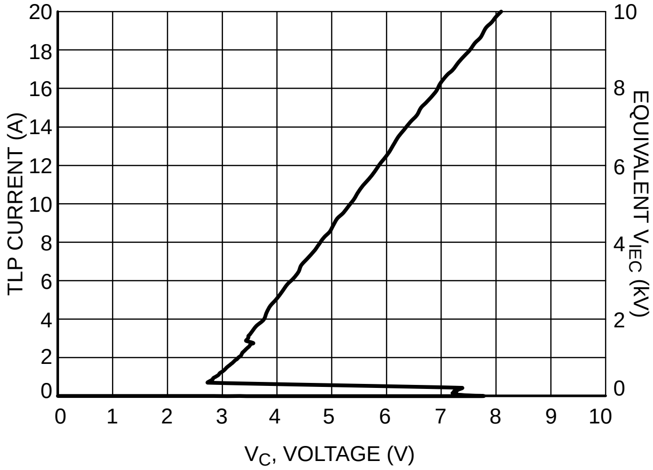


Figure 5. Positive TLP IV Curve

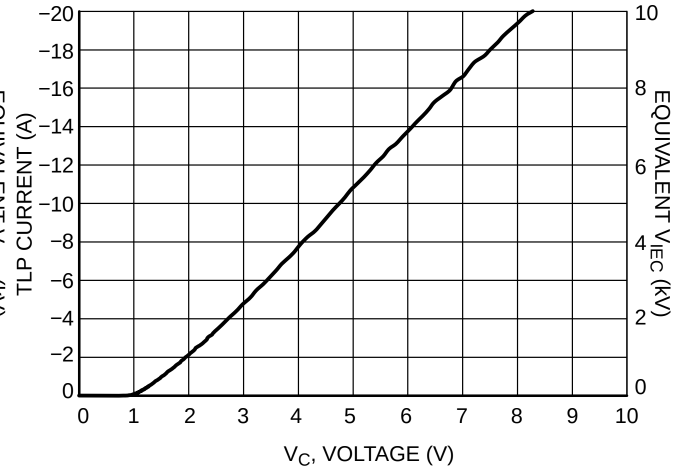


Figure 6. Negative TLP IV Curve

NOTE: TLP parameter: $Z_0 = 50\ \Omega$, $t_p = 100$ ns, $t_r = 300$ ps, averaging window: $t_1 = 30$ ns to $t_2 = 60$ ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

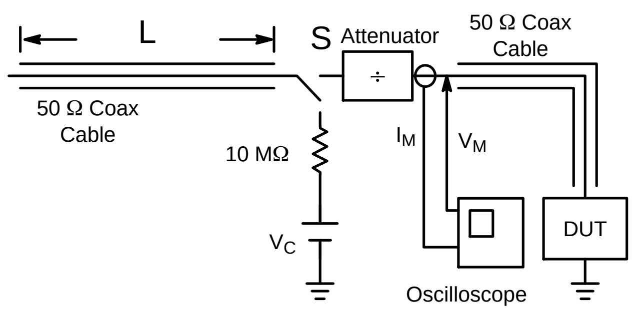


Figure 7. Simplified Schematic of a Typical TLP System

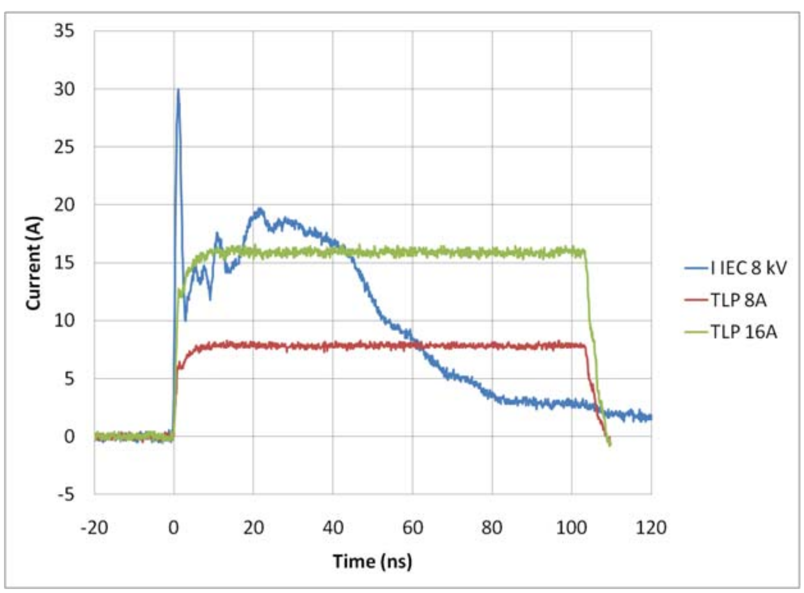


Figure 8. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

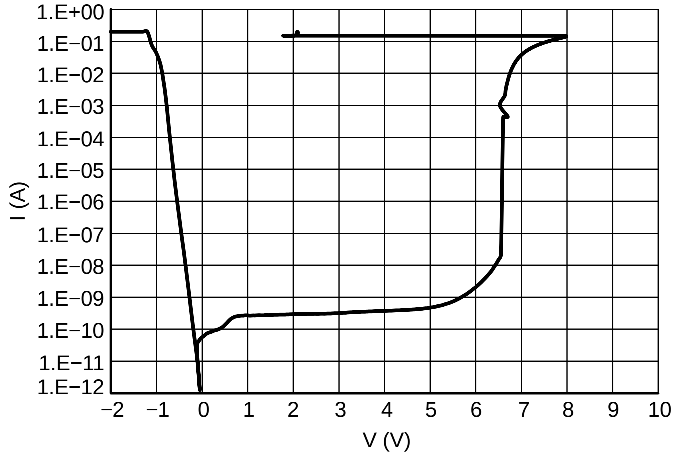


Figure 9. IV Characteristics

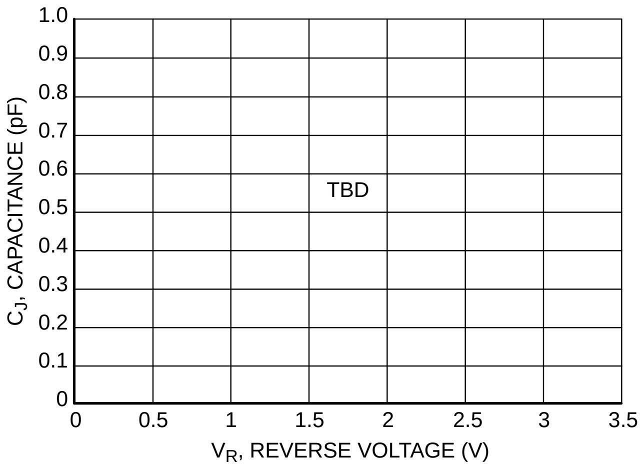


Figure 10. CV Characteristics

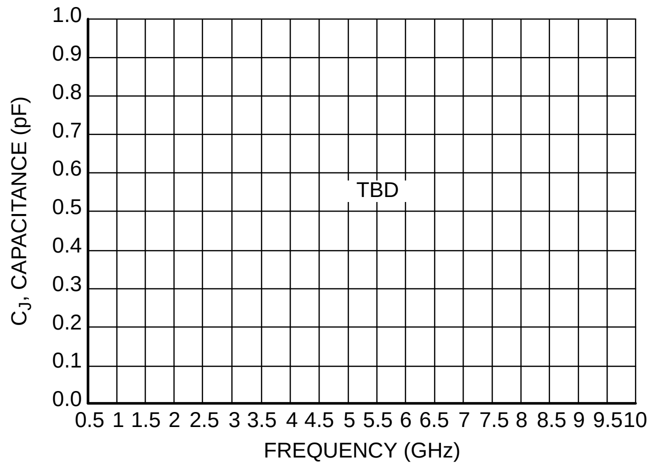


Figure 11. Junction Capacitance vs. Frequency

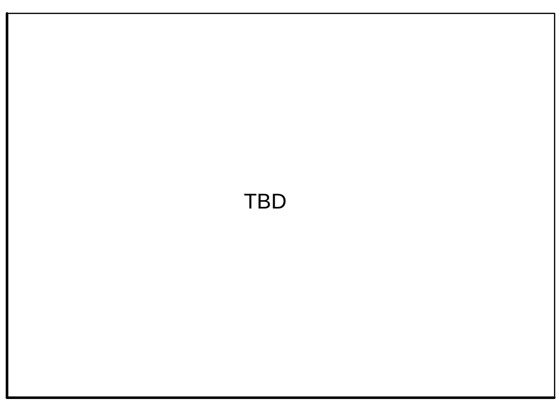
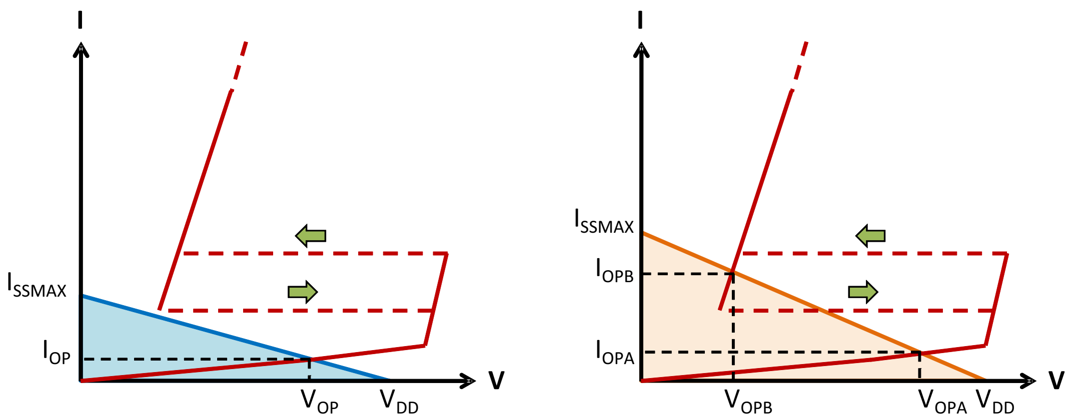


Figure 12. ESD9101 Insertion Loss

Latch-Up Considerations

ON Semiconductor's 9100 series of ESD protection devices utilize a snap-back, SCR type structure. By using this technology, the potential for a latch-up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch-up free applications and applications with the potential for latch-up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch-up free load line case, the IV characteristic of the snapback protection device intersects the load-line in one unique point (V_{OP}, I_{OP}). This is the only stable operating point of the circuit and the system is therefore latch-up free. In the non-latch up free load line case, the IV characteristic of the snapback protection device intersects the load-line in two points (V_{OPA}, I_{OPA}) and (V_{OPB}, I_{OPB}). Therefore in this case, the potential for latch-up exists if the system settles at (V_{OPB}, I_{OPB}) after a transient. Due to its high holding current, the ESD9101 is suitable for HDMI and 5 V active antenna applications where previous ESD8000 series devices were not. ***When designing this part into the application, please note the latch−up considerations by performing a loadline analysis corresponding to the data line and ESD9101's SCR characteristics.*** For a more in-depth explanation of latch-up considerations please refer to Application Note AND9116/D.



Latch−up Free Condition

Potential Latch−up Condition

Figure 13. Example Load Lines for Latch−up Free Applications and Applications with the Potential for Latch-up

Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH-UP FREE APPLICATIONS

Application	VBR (min) (V)	IH (min) (mA)	VH (min) (V)
HDMI 1.4/1.3a TMDS	3.465	54.78	1.0
USB 2.0 LS/FS	3.301	1.76	1.0
USB 2.0 HS	0.482	N/A	1.0
USB 3.0/3.1 SS	2.800	N/A	1.0
DisplayPort	3.600	25.00	1.0
GPS (Active)	5.200	80.00	1.0

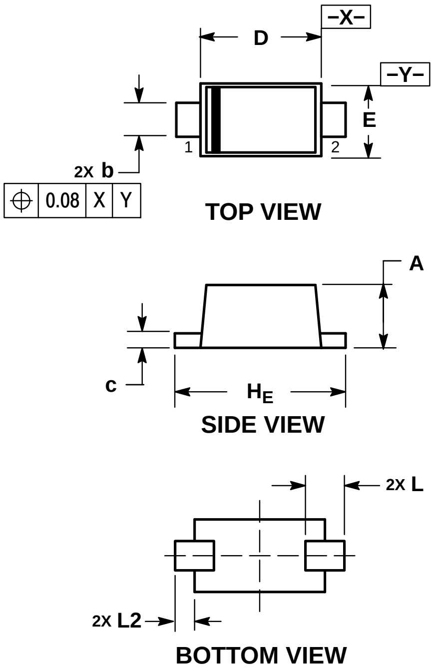
ORDERING INFORMATION

Device	Package	Shipping†
ESD9101P2T5G	SOD−923 (Pb−Free)	8000 / Tape & Reel
SZESD9101P2T5G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

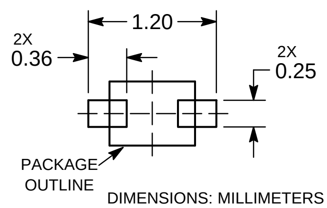
SOD−923
CASE 514AB−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H_E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.19 REF			0.007 REF		
L2	0.05	0.10	0.15	0.002	0.004	0.006

SOLDERING FOOTPRINT*



See Application Note AND8455/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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