CMOS 1.8 V to 5.5 V, 2.5 Ω 2:1 Mux/SPDT Switch in SOT-23

ADG719-EP

FEATURES

1.8 V to 5.5 V single supply
4 Ω (max) on resistance
0.75 Ω (typ) on resistance flatness
−3 dB bandwidth > 200 MHz
Rail-to-rail operation
6-lead SOT-23 package
Fast switching times:
  t_{ON} = 12 ns
  t_{OFF} = 6 ns
Typical power consumption: (< 0.01 µW)
TTL/CMOS compatible
Military temperature range: −55°C to +125°C

APPLICATIONS

Battery-powered systems
Communication systems
Sample-and-hold systems
Audio signal routing
Video switching
Mechanical reed relay replacement

FUNCTIONAL BLOCK DIAGRAM

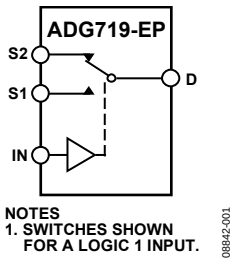

Figure 1.

GENERAL DESCRIPTION

The ADG719-EP is a monolithic CMOS SPDT switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

The ADG719-EP can operate from a single-supply range of 1.8 V to 5.5 V, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc.

Each switch of the ADG719-EP conducts equally well in both directions when on. The ADG719-EP exhibits break-before-make switching action.

Because of the advanced submicron process, −3 dB bandwidths of greater than 200 MHz can be achieved.

The ADG719-EP is available in a 6-lead SOT-23 package.

Full details about this enhanced product are available in the ADG719 data sheet, which should be consulted in conjunction with this data sheet.

PRODUCT HIGHLIGHTS

1. Supports defense and aerospace applications (AQEC standard).
2. Military temperature range: −55°C to +125°C.
3. Controlled manufacturing baseline.
4. One assembly and test site.
5. One fabrication site.
6. Enhanced product change notification.
7. Qualification data available on request.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

4/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V.

Table 1.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA;
	4	7	Ω max	see Figure 13
On Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.5	Ω max	
LEAKAGE CURRENTS I_S (Off)				V_{DD} = 5.5 V
Source Off Leakage	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	1	nA max	see Figure 14
Channel On Leakage I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 1 V or V_S = V_D = 4.5 V;
	±0.25	5	nA max	see Figure 15
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	7		ns typ	R_L = 300 Ω, C_L = 35 pF
		12	ns max	V_S = 3 V; see Figure 16
t_{OFF}	3		ns typ	R_L = 300 Ω, C_L = 35 pF
		6	ns max	V_S = 3 V; see Figure 16
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF,
		1	ns min	V_{S1} = V_{S2} = 3 V; see Figure 17
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 18
Channel-to-Channel Crosstalk	−62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Bandwidth −3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 20
C_S (Off)	7		pF typ	
C_D, C_S (On)	27		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
				Digital inputs = 0 V or 5.5 V
I_{DD}	0.001		μA typ	
		1.0	μA max	

[1] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V.

Table 2.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH		0 V to V_{DD}	V	
Analog Signal Range				
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA;
		12	Ω max	see Figure 13
On Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		2.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source Off Leakage I_S (Off)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	1	nA max	see Figure 14
Channel On Leakage I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 1 V or V_S = V_D = 3 V;
	±0.25	5	nA max	see Figure 15
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	10		ns typ	R_L = 300 Ω, C_L = 35 pF
		15	ns max	V_S = 2 V; see Figure 16
t_{OFF}	4		ns typ	R_L = 300 Ω, C_L = 35 pF
		8	ns max	V_S = 2 V; see Figure 16
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 2 V; see Figure 17
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 18
Channel-to-Channel Crosstalk	−62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Bandwidth −3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 20
C_S (Off)	7		pF typ	
C_D, C_S (On)	27		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
				Digital inputs = 0 V or 3.3 V
I_{DD}	0.001		μA typ	
	1.0		μA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-23 Package	
θ_{JA} Thermal Impedance[2]	186.45°C/W
Lead Soldering	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec
ESD	1 kV

[1]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given
[2]Measured on a 4-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

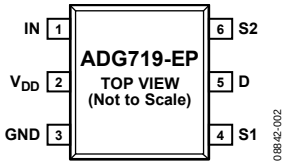

Figure 2. 6-Lead SOT-23 Pin Configuration

Table 4. Pin description

Pin No.	Mnemonic	Description
1	IN	Digital Switch Control Pin.
2	VDD	Most Positive Power Supply Pin.
3	GND	Ground (0 V) Reference Pin.
4	S1	Source Terminal. Can be used as an input or output.
5	D	Drain Terminal. Can be used as an input or output.
6	S2	Source Terminal. Can be used as an input or output.

Table 5. Truth Table

ADG719-EP IN	Switch S1	Switch S2
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

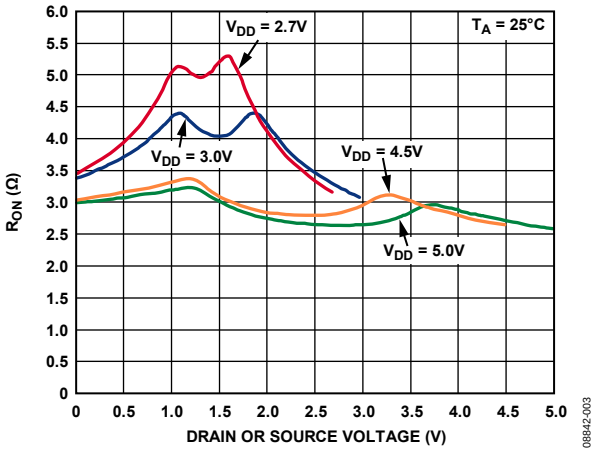

Figure 3. On Resistance vs. V_D (V_S), Single Supplies

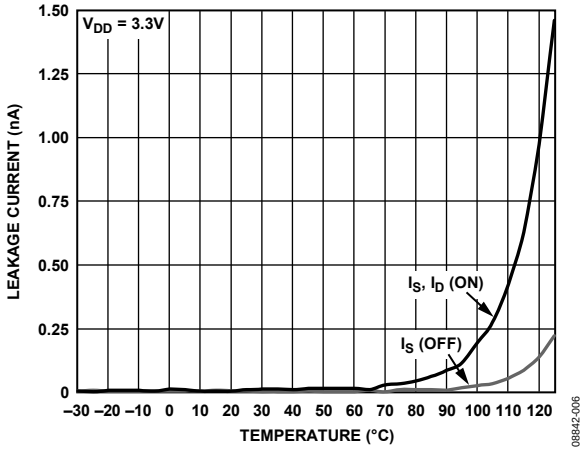

Figure 6. Leakage Currents vs. Temperature

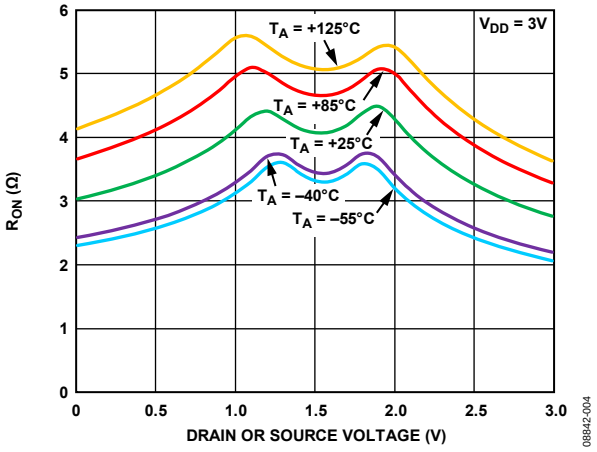

Figure 4. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 3 V

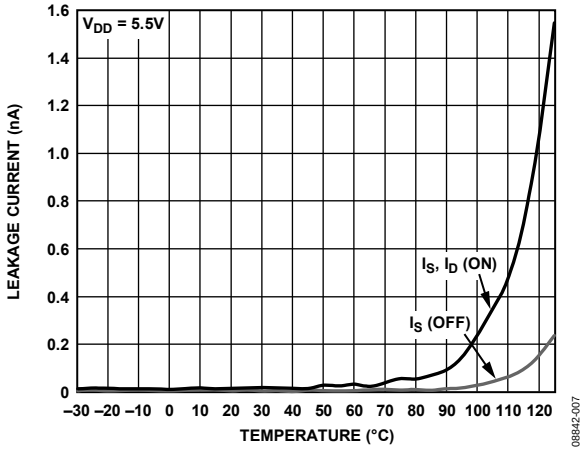

Figure 7. Leakage Currents vs. Temperature

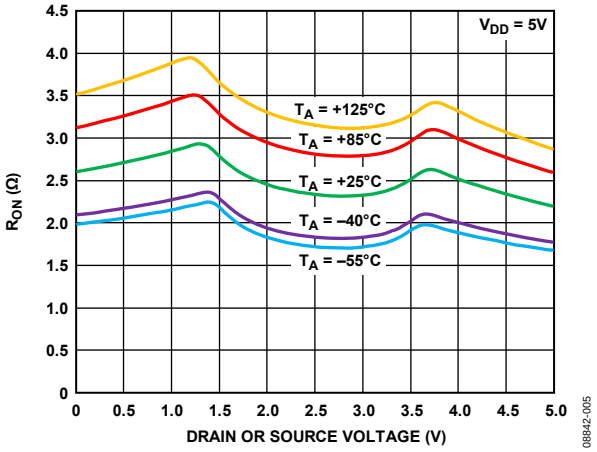

Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 5 V

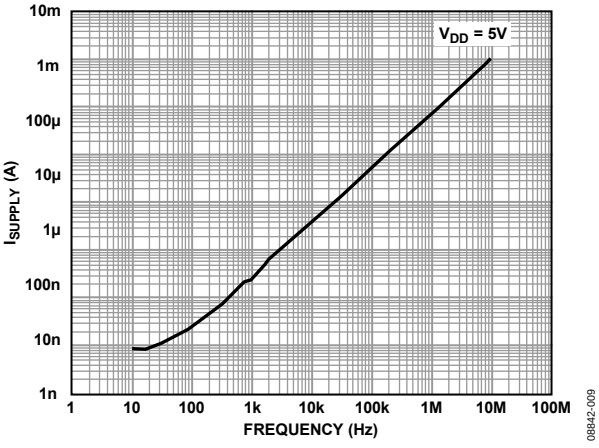

Figure 8. Supply Current vs. Input Switching Frequency

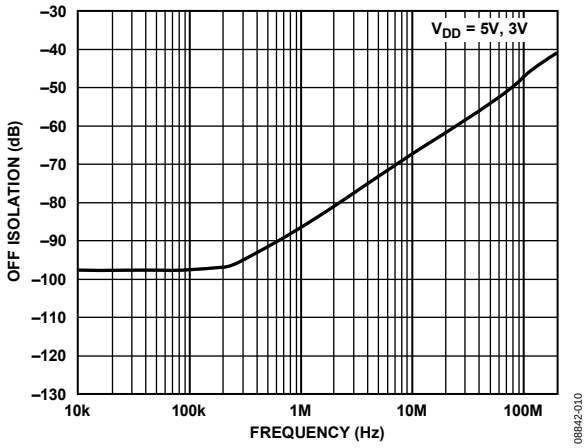

Figure 9. Off Isolation vs. Frequency

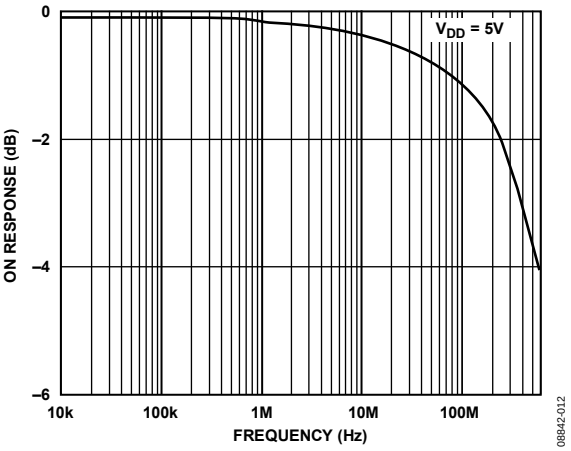

Figure 11. On Response vs. Frequency

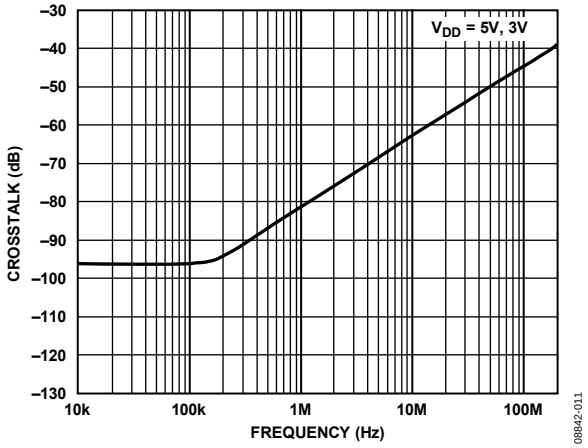

Figure 10. Crosstalk vs. Frequency

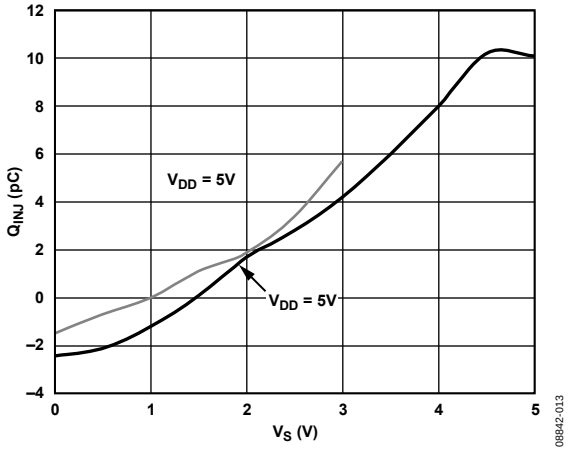

Figure 12. Charge Injection vs. Source Voltage

TEST CIRCUITS

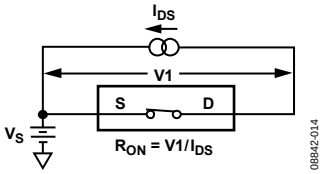

Figure 13. On Resistance

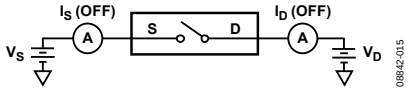

Figure 14. Off Leakage

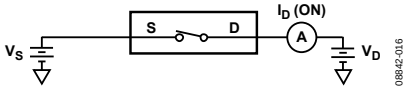

Figure 15. On Leakage

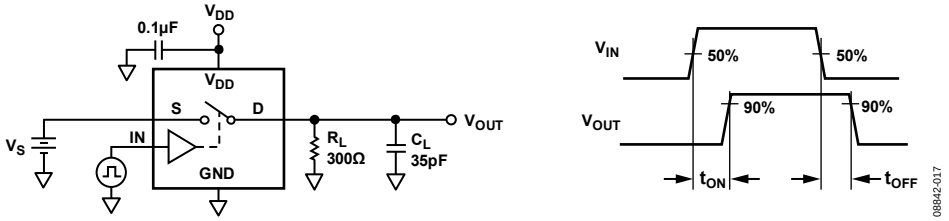

Figure 16. Switching Times

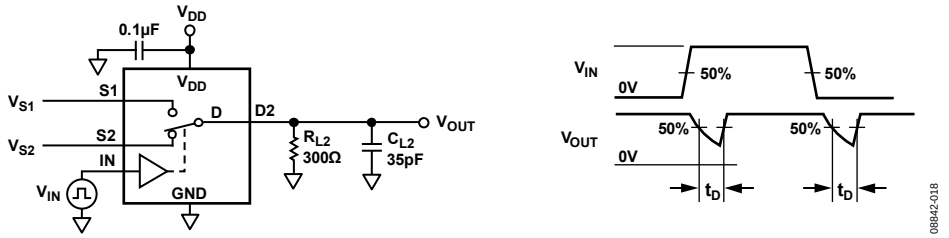

Figure 17. Break-Before-Make Time Delay, t_D

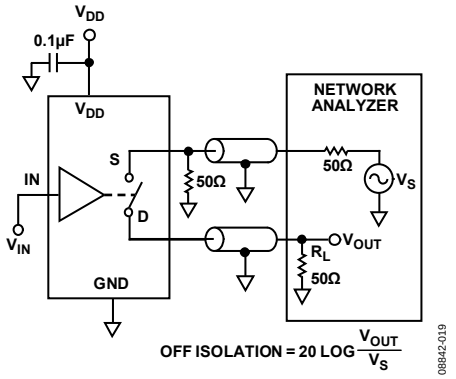

Figure 18. Off Isolation

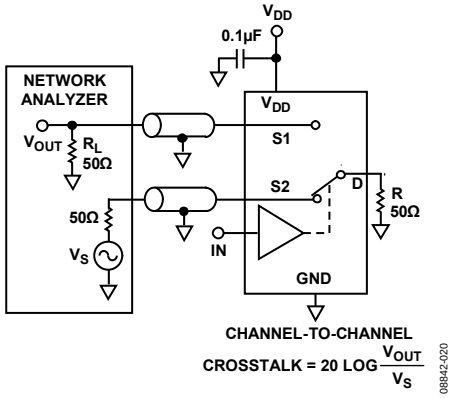

Figure 19. Channel-to-Channel Crosstalk

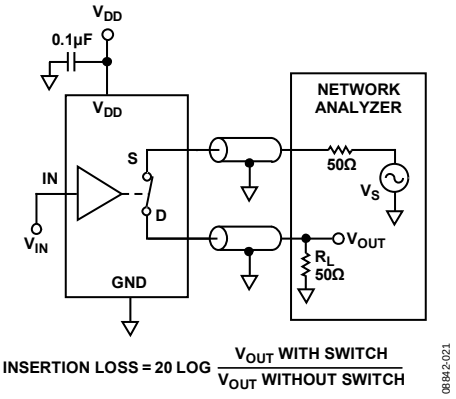

Figure 20. Bandwidth

OUTLINE DIMENSIONS

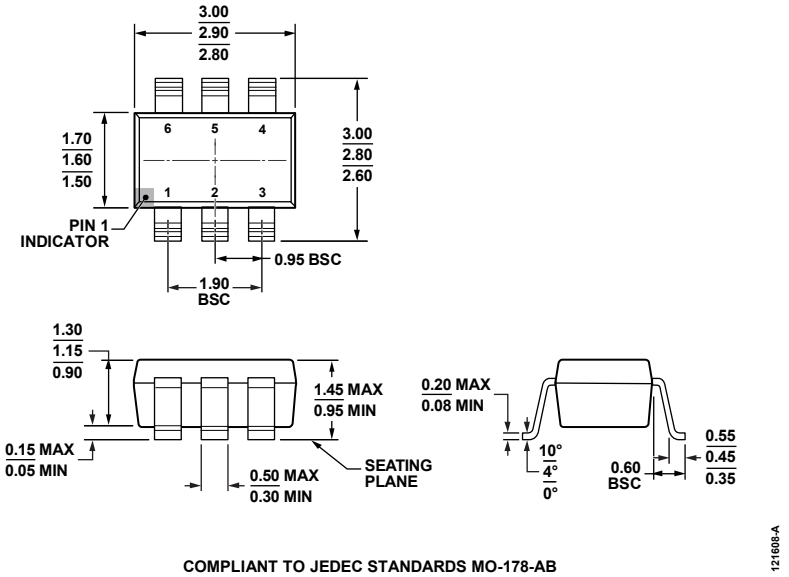

Figure 21. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG719SRJZ-EP-RL7	−55°C to +125°C	6-Lead SOT-23	RJ-6	S3T

[1] Z = RoHS Compliant Part.

NOTES

D08842-0-4/10(0)