NCP5030

Buck-Boost Converter to Drive a Single LED from 1 Li-Ion or 3 Alkaline Batteries

The NCP5030 is a fixed frequency PWM buck−boost converter optimized for constant current applications such as driving high−powered white LED. The buck−boost is implemented in an H−bridge topology and has an adaptive architecture where it operates in one of three modes: boost, buck−boost, or buck depending on the input and output voltage condition. This device has been designed with high−efficiency for use in portable applications and is capable of driving in DC up to 900 mA into a high power LED for flashlight / torch applications. To protect the device cycle−by−cycle current limiting and a thermal shutdown circuit have been incorporated as well as output over−voltage protection. The 700 kHz switching frequency allows the use of a low value 4.7 μH and ceramic capacitors. The NCP5030 is housed in a low profile space efficient 3x4 mm thermally enhanced WDFN.

Features

- Efficiency: 87% at 500 mA and 3.3 V V_{IN}
- Internal Synchronous Rectifier, No Schottky Diodes
- Adjustable Switching Limit Current to Optimize inductor size
- 0.3 μA Shut−down Control with “True−Cut off”
- Input Voltage Range from 2.7 V to 5.5 V
- 200 mV Feedback Voltage
- Output Over−voltage and Thermal Shut Down Protection

Typical Applications

- Portable Flashlight / Torch Lights

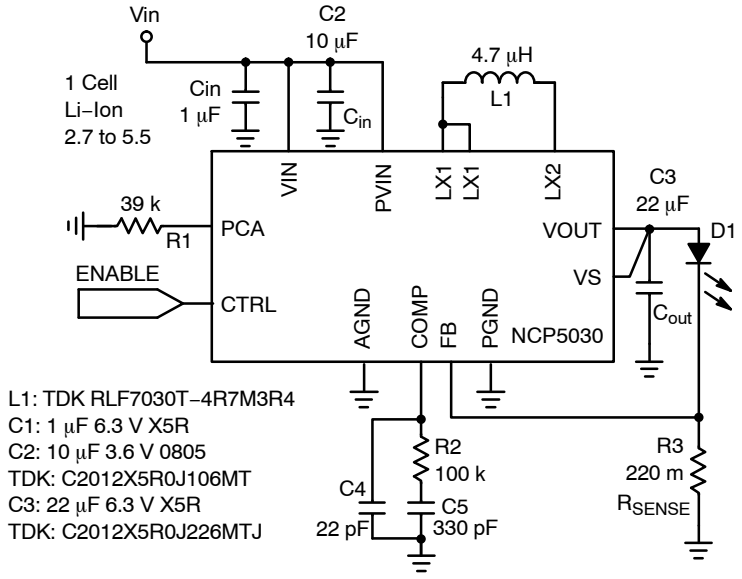

Figure 1. Typical Application Circuit

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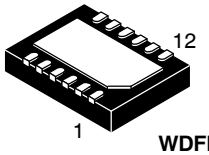
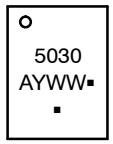


WDFN12 3x4
MT SUFFIX
CASE 506AY

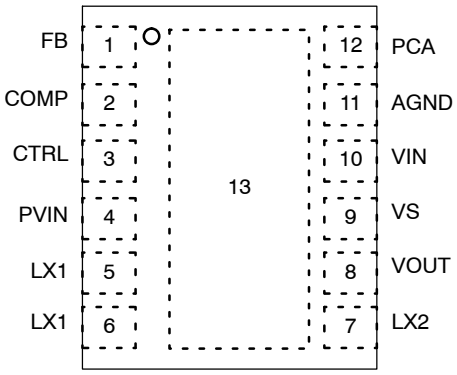
MARKING DIAGRAM



5030	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

Exposed pad (Pin 13) is PGND must be soldered to PCB GND plane

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

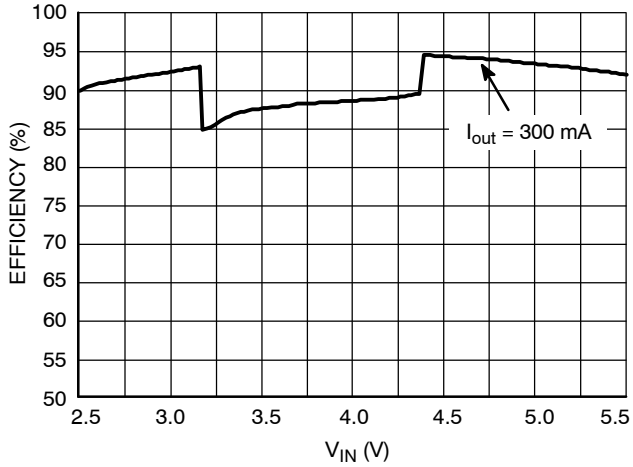


Figure 2. Efficiency vs. V_{in} Voltage

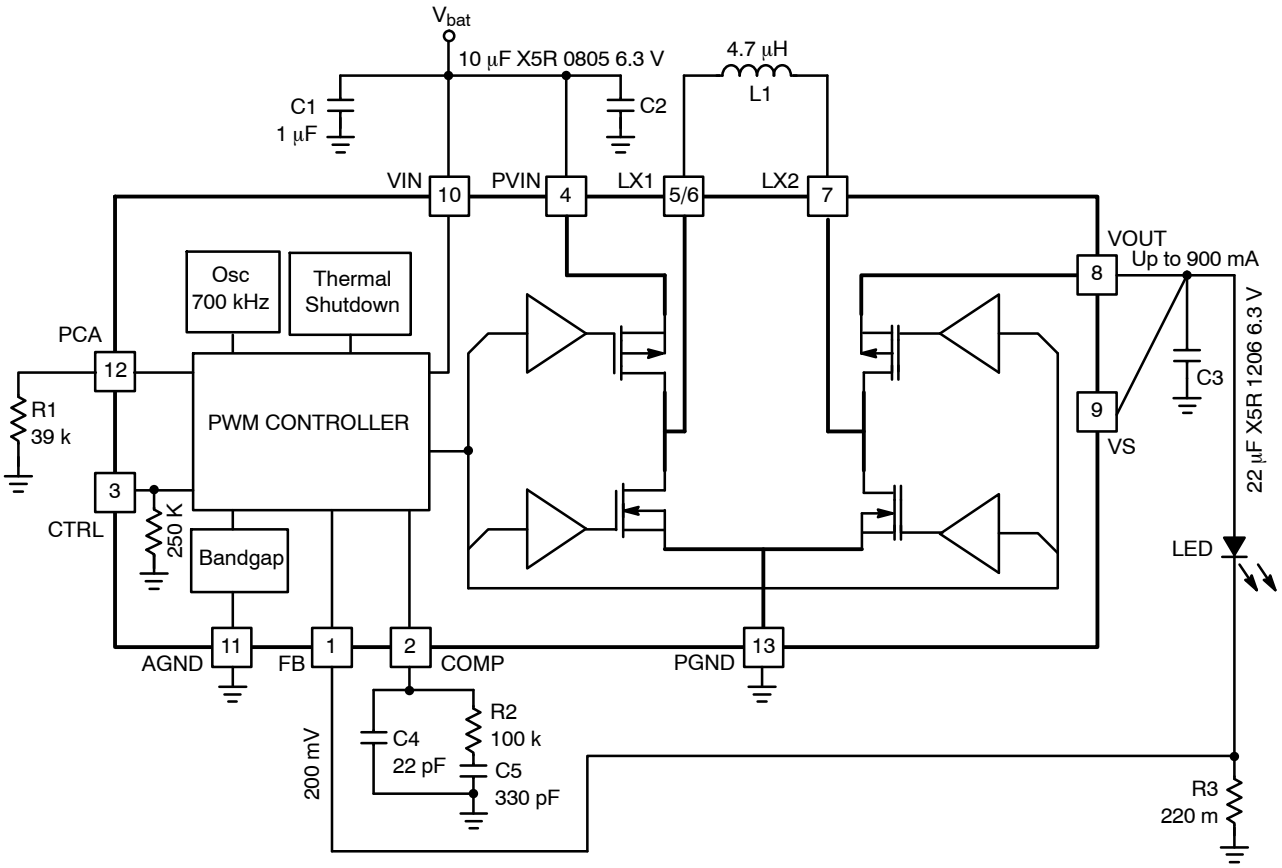


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
1	FB	INPUT	**Feedback:** Reference voltage is 200 mV. The cathode of the LED and a resistor to ground to set the LED current should be connected at this point. A ±5% metal film resistor, or better, is recommended for best output accuracy. An analog signal can be applied to this input to dim the LED.
2	COMP	INPUT	**Loop Compensation:** A frequency compensation network must be connected between this pin to the ground to ensure the stability of the closed loop. See “loop compensation” guidelines.
3	CTRL	INPUT	**Control and Enable:** An active High logic level on this pin enables the device. A built−in pulldown resistor disables the device if the input is left open. This pin can also be used to control the average current into the load by applying a low frequency PWM signal. If a PWM signal is applied, the frequency should be high enough to avoid optical flicker, but be no greater than 1.0 kHz.
4	PVIN	POWER	**Power Voltage Input Supply:** A 10 μF ceramic capacitor or larger must bypass this input to the ground. This capacitor should be placed as close a possible to this input.
5/6	LX1	POWER	**Switch LX1:** Both pins are connected to the input node of the H−bridge. The inductor should be connected between this node and LX2. The recommended inductor size is 4.7 μH.
7	LX2	POWER	**Switch LX2:** This pin is connected to the opposite node of the H−bridge and the power inductor is connected between this node and LX1.
8	VOUT	POWER	**Power Output:** A filter capacitor is necessary on this pin for the stability of the loop, to smooth the current flowing into the load, and to limit the noise created by the fast transients present in this circuitry. A 22 μF ceramic capacitor bypass to GND or larger is recommended. For White LED applications, this pin is also connected to the anode of the LED. Care must be observed to avoid EMI through the PCB copper tracks connected to this pin.
9	VS	POWER	**Voltage Sense:** This pin must be connected to C_{OUT} with a dedicated track to minimize serial parasitic inductor and to sense V_{OUT} with high accuracy. This pin supplies some of the NCP5030 internal blocks when the voltage is higher than V_{IN}.
10	VIN	POWER	**Supply Pin:** This pin supplies the internal control circuitry and must be connected to PVIN. Recommended bypass capacitor is 1.0 μF ceramic or larger.
11	AGND	POWER	**Analog Ground:** This pin is the system ground and carries the analog signals. This pin must be connected to the ground plan like PGND.
12	PCA	INPUT	**Peak Current Adjust:** A resistor between this input and ground controls the maximum peak current allowed in the inductor. The minimum value for this resistor is 30 kΩ. Increasing this value decreases the peak current. This allows the user to adjust the current based on the application needs and scale the size of the inductor accordingly. See “Switch Current Limit“guidelines in application section.
13	PGND	POWER	**Power Ground:** This pin is the power ground for NCP5030 and carries the switching current. Care must be observed to avoid high−density current flow in a limited PCB copper track.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 2)	V_{bat}	7.0	V
Over Voltage Protection	V_{out}	6.5	V
Human Body Model (HBM) ESD Rating (Note 3)	ESD HBM	2.0	kV
Machine Model (MM) ESD Rating (Note 3)	ESD MM	200	V
Digital Input Voltage Digital Input Current	CTRL	$-0.3 < V_{in} < V_{bat} + 0.3$ 1.0	V mA
WDFN 3x4 Package Power Dissipation @ T_A = +85°C (Note 5) Thermal Resistance, Junction−to−Case Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JC}$ $R_{\theta JA}$	 Internally Limited 6.0 (Note 6)	 W °C/W °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Moisture Sensitivy Level (Note 7)	MSL	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins
4. Latchup Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
5. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation.
6. For the 12−Pin 3x4 WDFN Package, the $R_{\theta JA}$ is highly dependent on the PCB heat−sink area. For example, $R_{\theta JA}$ can be 57°C/W for a one layer board and 43 for a four layer board.
7. Per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (Limits apply for T_A between −40°C to +85°C and V_{in} = 3.6 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operational Power Supply	V_{IN}	2.7	–	5.5	V
Maximum Inductor Current (Note 11) (See Figure 8)	I_{PEAK_MAX}	−20%	4.0	+20%	A
Switches P1 and P2 ON Resistance	P_{MOS} R_{DSON}	–	100	–	mΩ
Switches N1 and N2 ON Resistance	N_{MOS} R_{DSON}	–	100	–	mΩ
Switches P1 and P2 Leakage Current	P_{MOS} L	–	0.5	–	μA
Switches N1 and N2 Leakage Current	N_{MOS} L	–	0.5	–	μA
Internal Oscillator Frequency (Note 8)	F_{OSC}	600	700	800	kHz
Efficiency (Notes 9, 10 and 11)	E_{FF}	–	85	–	%
Output Voltage Range (Note 11)	V_{OUT}	2.2	–	5.5	V
V_{OUT}–V_{IN} Threshold to Change Mode from Boost to Buck–Boost	T_{BOOST}	–	375	–	mV
V_{IN}–V_{OUT} Threshold to Change Mode from Buck–Boost to Buck	T_{BUCK}	–	650	–	mV
Threshold to Change Mode Hysteresis	H_{MODE}	–	100	–	mV
Available Output Power (Note 11) When $V_{in} \geq 3.1$ V (V_{out} = 4.7 V, 900 mA)	P_{OUT}	4.3	–	–	W
Feedback Voltage Threshold in Steady State at 25°C	F_{BV}	190	200	210	mV
Line Regulation, Measured on FB Pin (Note 8) From DC to 100 Hz and R_{FB} = 1 Ω	F_{BVLR}	–	5.0	–	mV/V
Feedback Input Current	F_{BC}	–	–	0.1	μA
Standby Current at I_{OUT} = 0 mA, CTRL = Low, V_{bat} = 4.2 V	I_{STB}	–	0.3	3.0	μA
Quiescent Current Switching at I_{OUT} = 0 mA, CTRL = High, V_{bat} = 4.2 V (Note 12)	I_{QS}	–	5.0	–	mA
V_{IN} Undervoltage Lockout Threshold to Enable the Converter	U_{VLO}	2.2	2.4	2.6	V
Undervoltage Lockout Hysteresis	U_{VLOH}	–	100	–	mV
Soft−start Time (Note 11)	S_{ST}	–	1000	–	μs
Limit of CTRL pin PWM Dimming Frequency (Note 11)	F_{DIM}	–	0.2	–	kHz
Thermal Shutdown Protection	T_{SD}	–	160	–	°C
Thermal Shutdown Protection Hysteresis	T_{SDH}	–	20	–	°C
Voltage Input Logic Low	V_{IL}	–	–	0.4	V
Voltage Input Logic High	V_{IH}	1.2	–	–	V
CTRL Pin Pulldown Resistance	R_{CTRL}	150	220	290	kΩ

8. T_A between −10°C to +85°C
9. Efficiency is defined by 100 * (P_{out}/P_{in}) at 25°C. V_{in} = 3.3 V, I_{OUT} = 500 mA, Load = 1 LED (V_f = 3.9 V)
10. L = 4.7 μH (TDK RLF7030T−4R7M3R4), C_{out} = 22 μF X5R
11. Guaranteed by design and characterized.
12. The overall tolerance is dependent on the accuracy of the external resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

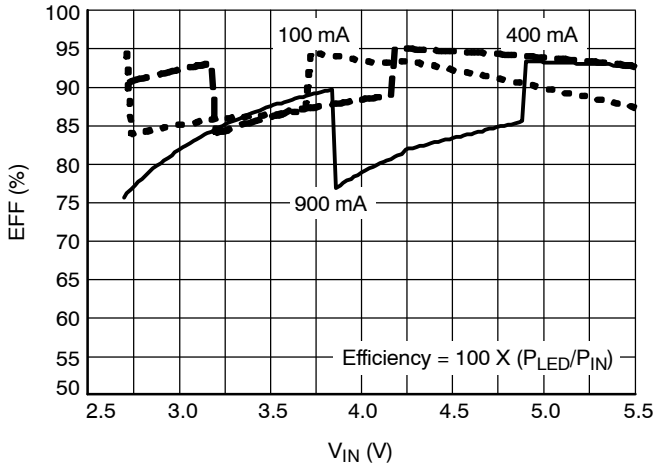


Figure 4. Efficiency vs. V_{IN} LED = Lumileds LUXEON III, L = TDK RLF7030T−4R7

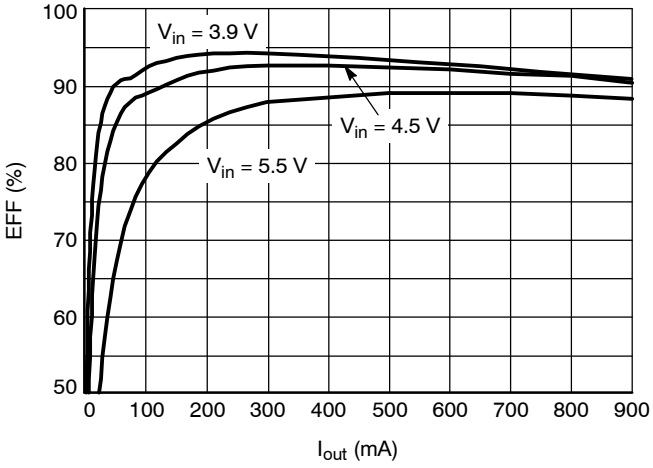


Figure 5. Buck Mode Efficiency vs. I_{OUT} @ V_{OUT} = 3.1 V L = TDK RLF7030T−4R7

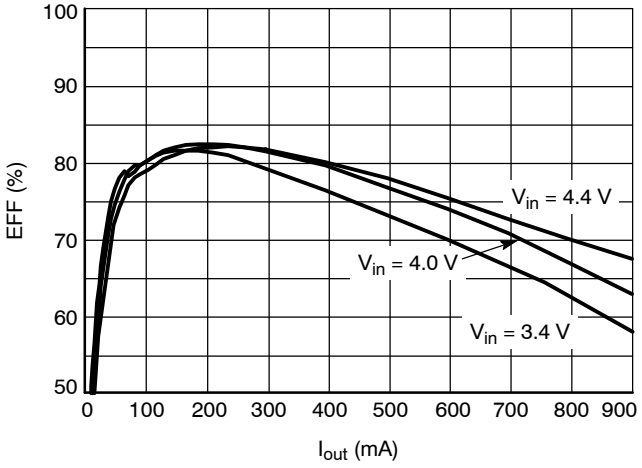


Figure 6. Buck−Boost Mode Eff. vs. I_{OUT} @ V_{OUT} = 3.8 V L = TDK RLF7030T−4R7

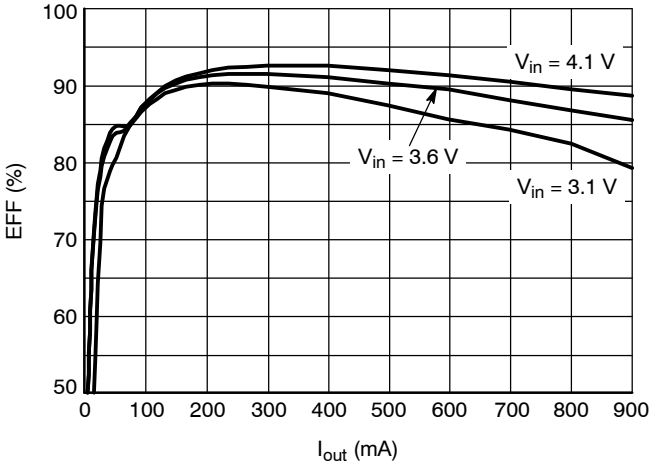


Figure 7. Boost Mode Efficiency vs. I_{OUT} @ V_{OUT} = 5.0 V L = TDK RLF7030T−4R7

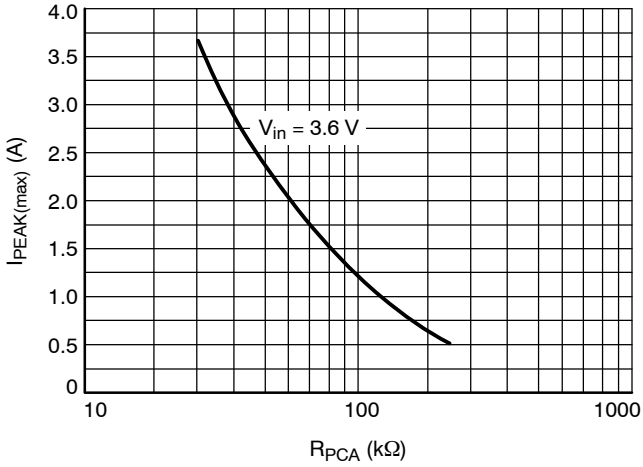


Figure 8. I_{PEAK_MAX} vs. R_{PCA}

TYPICAL PERFORMANCE CHARACTERISTICS

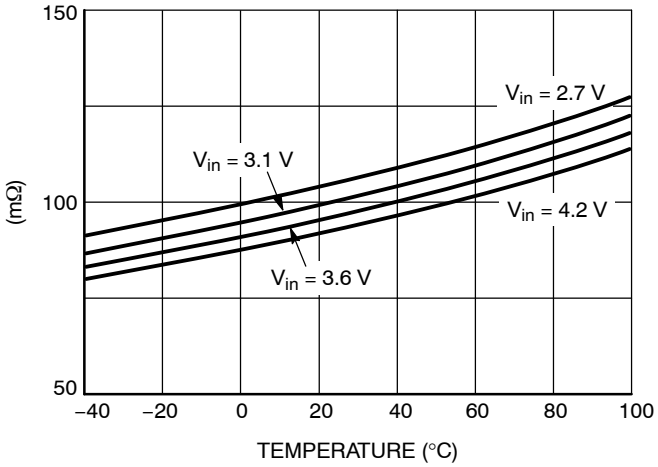


Figure 9. NMOS R_{DSON} vs. Temperature

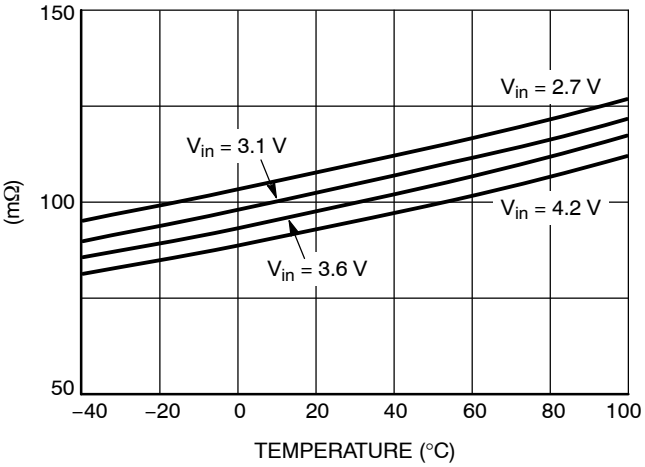


Figure 10. PMOS R_{DSON} vs. Temperature

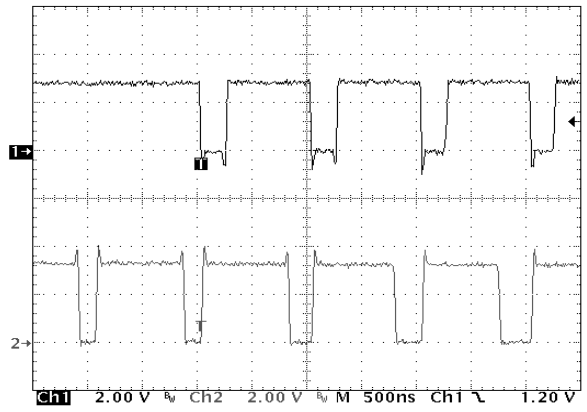


Figure 11. Transitional Period Switch Pins (LX1 and LX2) from Boost to Buck−Boost when V_{OUT} − V_{IN} is < than 375 mV

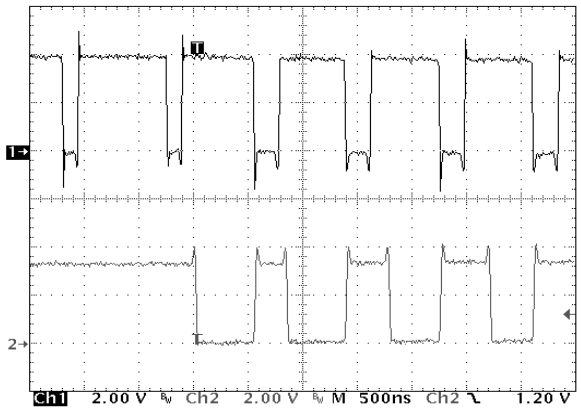


Figure 12. Transitional Period Switch Pins (LX1 and LX2) from Buck to Buck−Boost when V_{IN} − V_{OUT} is > than 650 mV

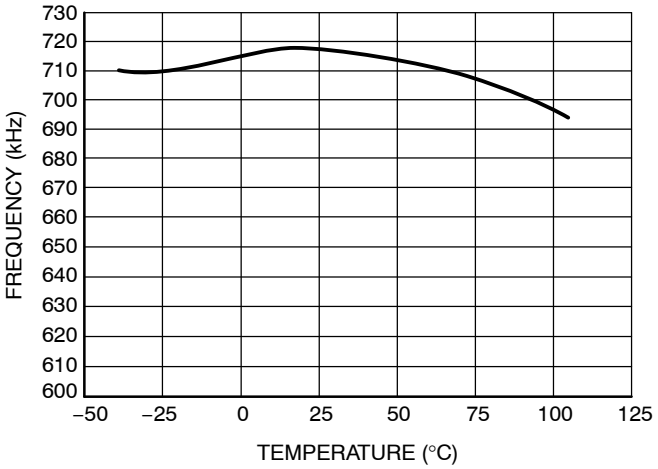


Figure 13. Oscillator Frequency vs. Temperature V_{OUT} = 3.6 V, V_{IN} = 3.6 V

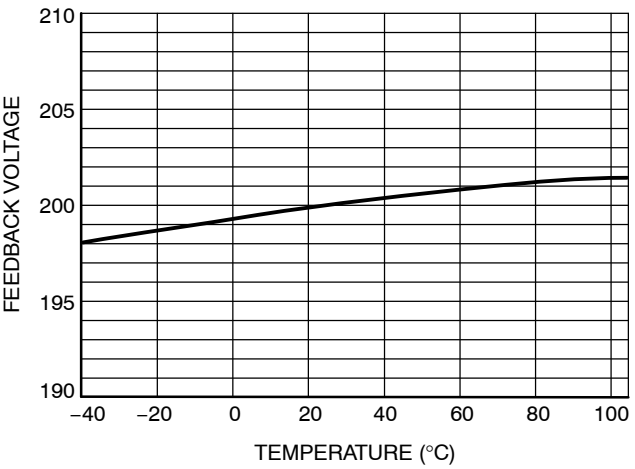


Figure 14. Feedback Voltage vs. Temperature V_{OUT} = 3.6 V, V_{IN} = 3.6 V

DETAILED OPERATING DESCRIPTION

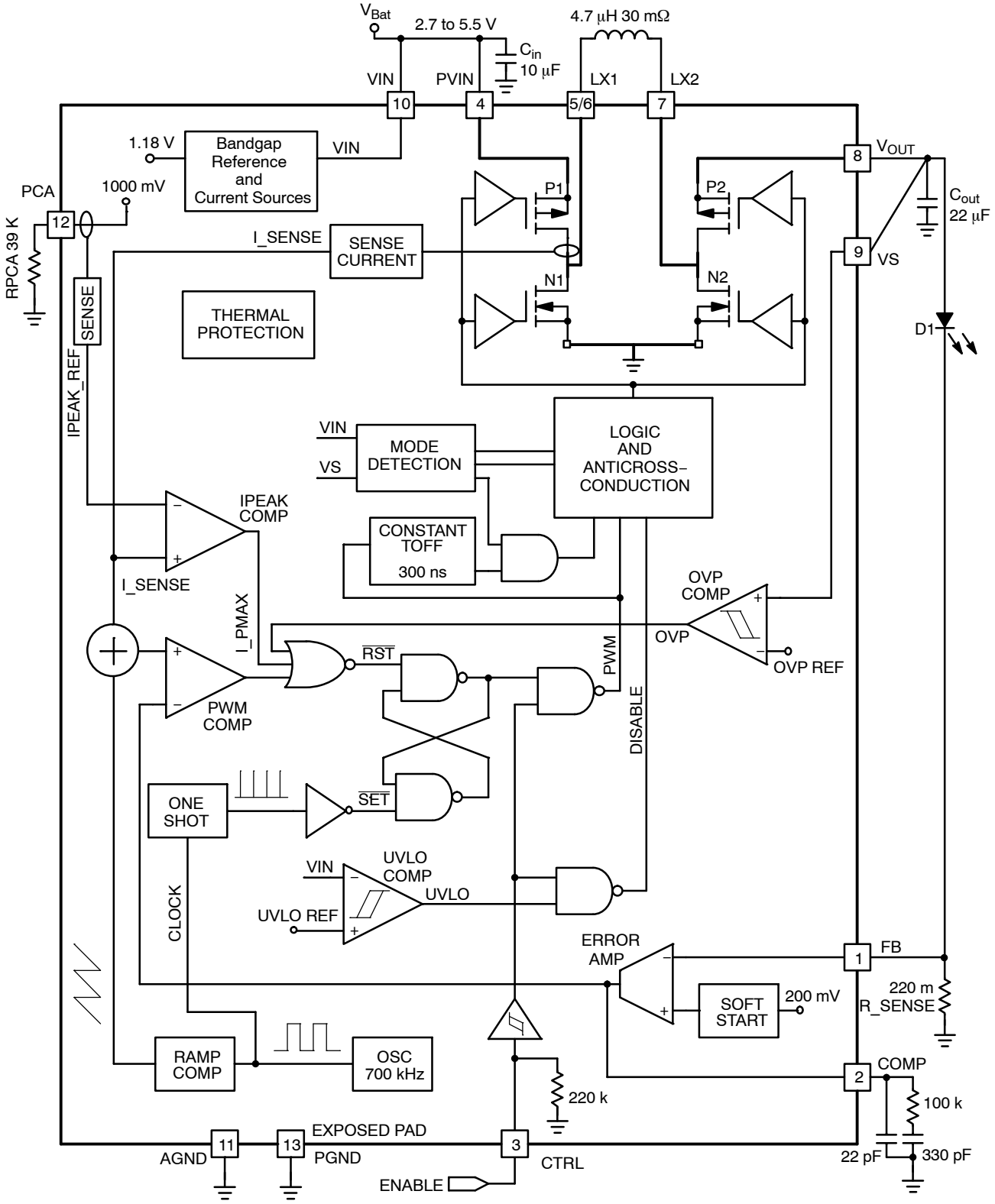


Figure 15. Functional Block Diagram

Operation

The NCP5030 DC−DC converter is based on a Current Mode PWM architecture specifically designed to efficiently provide a regulated current to a high current white LED. This device utilizes fixed frequency synchronous buck−boost switching regulator architecture. This topology is critical in single cell Lithium−Ion/ Polymer battery or 3 Alkaline powered applications as the forward voltage of the LED may be greater than or less than the battery voltage. A low feedback voltage of 200 mV (nom) minimizes power losses in the current setting resistor connected between the cathode of the LED and ground.

The core switching regulator is configured as a full bridge with four low R_{DSON} (0.1 Ω) MOSFET switches to maximize efficient power delivery. Another advantage of this topology is that it supports a true−shut down mode where the LED will be disconnected from the power supply when the device is placed in disable mode.

Figure 16 shows how the four switches are connected to charge and discharge the current from P_{VIN} to V_{OUT} through the inductor.

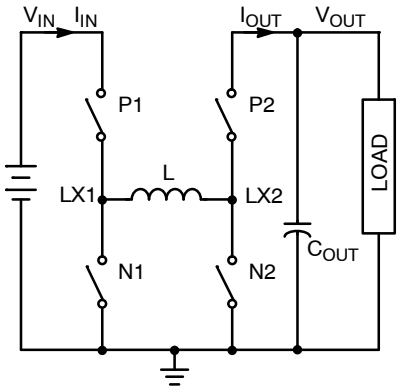


Figure 16. Basic Power Switches Topology

The converter operates in three different modes as a function of $V_{OUT} - V_{IN}$ (Figure 17): In Buck mode when V_{OUT} is below V_{IN} – 650 mV (T_{BUCK} nominal), in Boost mode when V_{OUT} is above V_{IN} + 375 mV (T_{BOOST} nominal) and in Buck−Boost mode when V_{OUT} is between this tow thresholds.

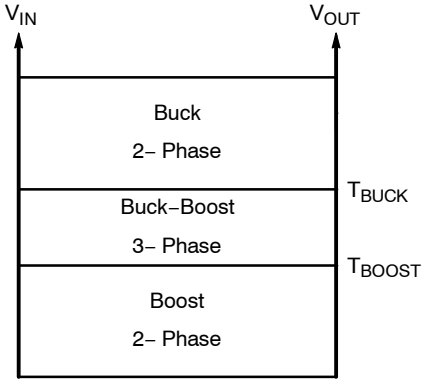


Figure 17. Conversion Mode

The internal oscillator provides a 700 kHz clock signal to trigger the PWM controller on each rising edge (SET signal) which starts a cycle. In pure buck or boost mode, the converter operates in two−phase mode, the first one to charge the inductor, followed by a synchronous rectifier discharge phase. However, in buck−boost mode, to get high efficiency the converter controls the switches in three separate phases (see Buck−Boost Mode Section). The capacitor C_{OUT} is used to store energy from the inductor to smooth output voltage thus constantly powering the load.

Buck Mode ($V_{OUT} < V_{IN} – 650$ mV)

In Buck mode, switches P1 and N1 are toggling and the two others are fixed, the switch N2 is all time OFF and the switch P2 is all time ON. The buck converter operates in two separate phase (See Figure 18). The first one is T_{ON} when $I_{IN} = I_{OUT}$. During this phase the switch P1 is ON, N1 is OFF and the current increases through the inductor. The switch current is measured by the SENSE CURRENT and added to the RAMP COMP signal. Then PWM COMP compares the output of the adder and the signal from ERROR AMP. When the comparator threshold is exceeded, T_{ON} phase is followed by T_{OFF}. P1 switch is turned OFF and N1 is ON until next clock rising edge. The current is only delivered by the inductor, which means that $I_{IN} = 0$

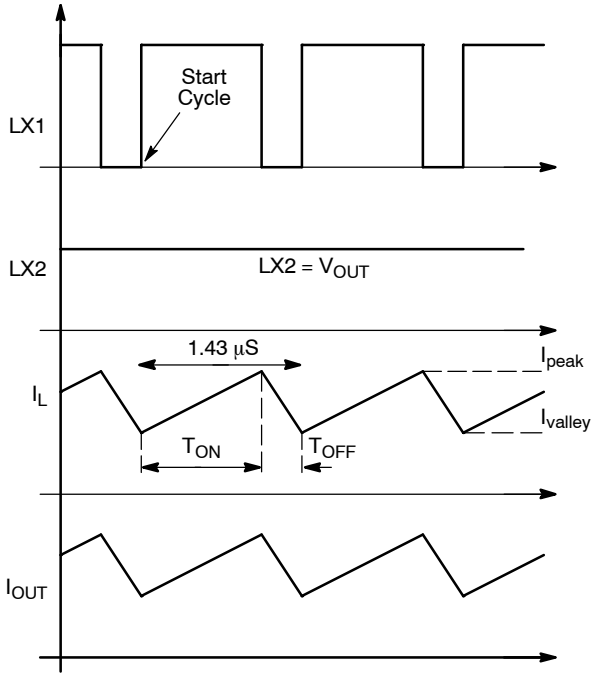


Figure 18. Basic DC−DC Buck Operation

Boost Mode ($V_{OUT} > V_{IN} + 375$ mV)

The switches in boost mode are inversely controlled than in buck mode. Switches P2 and N2 are toggling and the two others are fixed. Switch P1 is all time ON and the switch N1 is all time OFF. The boost converter operates in two separate phases (See Figure 19). The first one is T_{ON} when

the inductor is charged by current from the battery to store up energy. During this phase the switch N2 is on and P2 is off. The switch current is measured by the SENSE CURRENT and added to the RAMP COMP signal. Then PWM COMP compares the output of the adder and the signal from ERROR AMP. When the comparator threshold is exceeded, the flip−flop circuit is reset, P2 switch is turned on, and N2 is off until the rising edge of the next clock cycle.

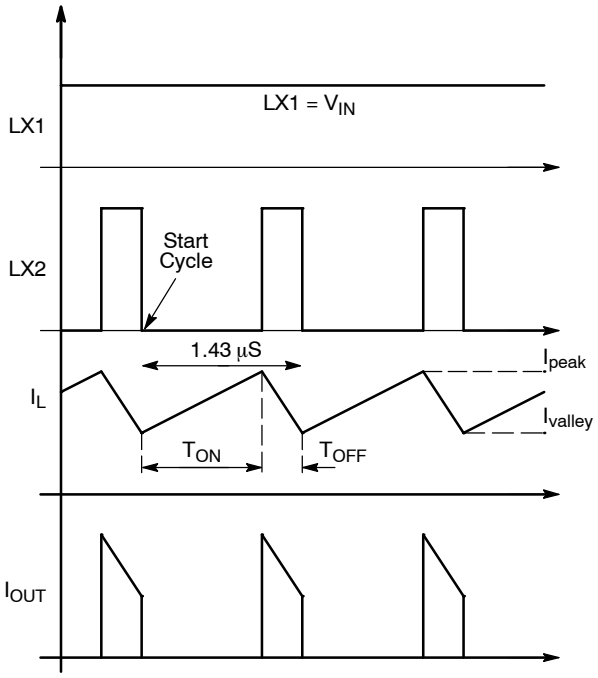


Figure 19. Basic DC−DC Boost Operation

Buck−Boost Mode
(V_{IN} – 650 mV < V_{OUT} < V_{IN} + 375 mV)

Figure 20 shows the basic DC−DC Buck−Boost operation. Now, all four switches are running and the controller operates in three separate phases to reach higher efficiency. The first step is T_{ON} when the inductor is charged by current from the battery. During this phase the switch P1_N2 are on and P2_N1 are off. Like the other modes, the current measured by SENSE CURRENT is added to the RAMP COMP signal and compared by PWM COMP with the signal from ERROR AMP. When PWM COMP threshold is exceeded, the flip−flop circuit is reset and the controller switches in T_{OFF} phase. In this second phase, the switch P1_N2 are off and P2_N1 are ON. Because time of T_{OFF} phase is constant, the current stored in the inductor during 250 ns (nominal) is drained to V_{OUT}. After this, CONSTANT T_{OFF} delay is over, the circuit logic switches in the third phase named TC (Time Conduction) where the inductor is directly connected from PVIN to V_{OUT}. The switch P1_P2 are on and switches N_N2 are off until the rising edge of the next clock cycle.

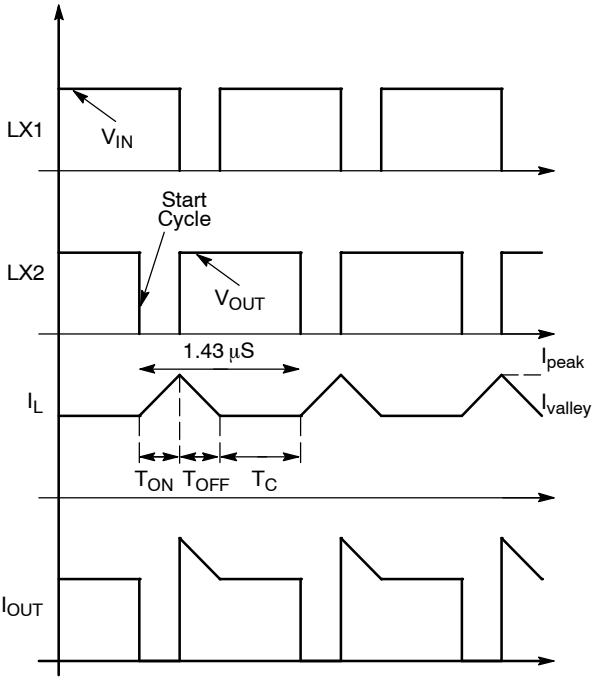


Figure 20. Basic DC−DC BB Operation

In addition, there are four safety circuits like OVP, UVLO, IPEAK COMP, THERMAL PROTECTION, which can disable the DC−DC conversion.

Error Amp and Compensation

Regulation loop is closed by the error amplifier, which compares the feedback voltage with the reference set at 200 mV. Thanks to the transconductance structure, the compensation network is directly connected to the error amplifier output. This external passive network is necessary to sets the dominant pole to gets a good loop stability. The compensation network shown in Figure 21 provides a phase margin greater than 45° whatever the current drives in a white LED load.

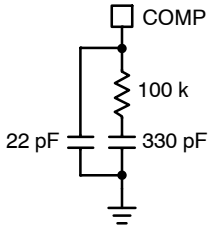


Figure 21. Compensation Network

LED Current Selection

The feedback resistor (R_{SENSE}) determines the LED current in steady state. The control loop regulates the current in such a way that the average voltage at the FB input is 200 mV (nominal). For example, should one need 800 mA output current, R_{SENSE} should be selected according to the following equation:

$$R_{SENSE} = \frac{F_{BV}}{I_{LED}} = \frac{200\ mV}{800\ mA} = 250\ m\Omega \qquad \text{(eq. 1)}$$

Current Selection

Figure 22 shows an application schematic to drive two selected currents I_1 and I_2.

$$I_{LED} = I_1 + I_2 \quad \text{(eq. 2)}$$

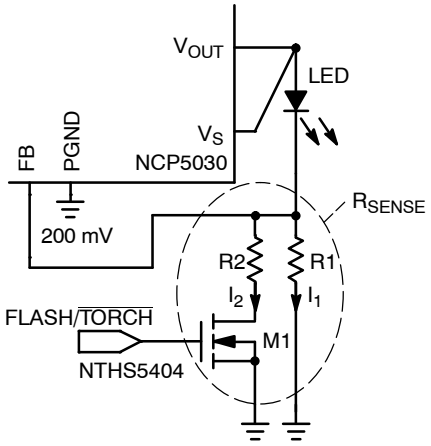


Figure 22. Two Current Selections

An active low logic level of M1 enables the low current mode, So $I_2 = 0$ and $I_1 = I_{LED} = 200\ mV / R_1$. For example, should one need 200 mA for low current mode and 800 mA for high current mode, R_1 should be selected according to the following below:

$$R_1 = \frac{F_{BV}}{I_1} = \frac{200\ mV}{200\ mA} = 1.0\ \Omega \quad \text{(eq. 3)}$$

So an active high logic level M1 on gate enables the high current mode then $I_{FLASH} = I_1 + I_2$ and according Equation 2 and 3, R2 should be selected regarding the following equation:

$$R_2 = \frac{F_{BV}}{I_{FLASH} - I_1} - R_{DSON\_M1}$$

$$R_2 = \frac{200\ mV}{800\ mA - 200\ mA} - 33\ m\Omega \quad \text{(eq. 4)}$$

$$R_2 = 300\ m\Omega$$

Some recommended resistors include, but are not limited to:

PANASONIC ERJ3BQF1R0V (1.0 Ω 1% 0603)

PANASONIC ERJ3BQFR30V (300 mΩ 1% 0603)

PANASONIC ERJ3BQJ1R0V (1.0 Ω 5% 0603)

PANASONIC ERJ3BQJR30V (300 mΩ 5% 0603)

Analogue Dimming

In white LED applications, it is desirable to operate the LEDs at a specific operating current, as the color shift as the bias current. As a consequence, it is recommended to dim the LED current by Pulse Width Modulation techniques. A low frequency PWM signal can be applied to the CTRL input. LED brightness can be changed by varying the duty cycle. To avoid any optical flicker the frequency must be higher than 100 Hz and preferably less than 300 Hz. Because of the soft−start function set at 1000 μs (nominal), higher frequency would cause the device to remain active with lower than expected brightness. Nevertheless, in this case a dimming control using a filtered PWM signal can be used. In addition, for DC voltage control the same technique is suitable and the filter is taken away. Please refer to “NPC5030 Dimming Control Application Note”.

Inductor Selection

Three main electrical parameters need to be considered when choosing an inductor: the value of the inductor, the saturation current and the DCR. Firstly, we need to check if the inductor is able to handle the peak current without saturating. Therefore, we have to consider that the maximum peak inductor current is in Buck−Boost mode when V_{OUT} is closed T_{BOOST} threshold for the lower operating V_{IN}. Obviously, the peak current inductor is higher when this device supplies the maximum required current. In this case, the DC−DC converter is supposed to operate in Continuous Conduction Mode (CCM) so the dotted curve in Figure 23 gives the inductor peak current as a function of load current:

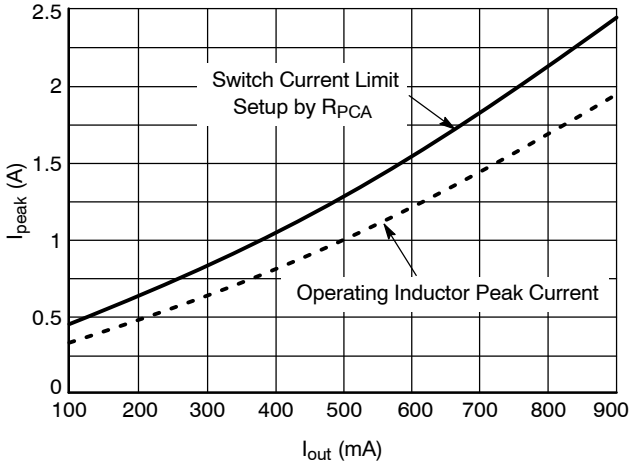


Figure 23. Inductor Peak Currents Vs. I_{OUT} (mA)

Finally, an acceptable DCR must be selected regarding losses in the coil and must be lower than 100 mΩ to limit excessive voltage drop. In addition, as DCR is reduced, overall efficiency will improve. Some recommended inductors are included but are not limited to:

TDK VLF5014AT−4R71R1

TDK RLF7030T−4R7M3R4

COPPER BUSSMANN FP3−4R7

MURATA LQH43CN4R7M03L

NIC: NIP16W4R7MTRF

Switch Current Limit

This safety feature is clamping the maximum allowed current in the inductor according to external R_{PCA} resistor, which is connected between PCA input and the ground. This allows the user to reduce the peak current being drawn

from the supply according to the application's specific requirements. The I_{peak} maximum value is 4 A, resulting in a minimum resistor value of 30 kΩ. Please refer to Figure 8 I_{PEAK_MAX} Vs R_{PCA} page 6 to choose R_{PCA} value versus I_{PEAK_MAX}. By limiting the peak current to the needs of the application, the inductor sizing can be scaled appropriately to the specific requirements. This allows the PCB footprint to be minimized.

Input and Output Capacitors Selection

C_{OUT} stores energy during the T_{OFF} phase and sustains the load current during the T_{ON} phase. In order ensure the loop stability and minimize the output ripple, at least 22 μF low ESR multi−layer ceramic capacitor type X5R is recommended.

The V_{IN} and PV_{IN} input pin need to be bypassed by a X5R or an equivalent low ESR ceramic capacitor. Near the PV_{IN} pin at least 10 μF 6.3 V or higher ceramic capacitor is needed. Regarding V_{IN} pin a 1 μF 6.3 V close to the pad is sufficient. Some recommended capacitors include but are not limited to:

22 μF 6.3 V 0805
TDK: C2012X5R0J226MTJ

22 μF 6.3 V 1206
MURATA: GRM31CR60J226KE19L

10 μF 6.3 V 0805
TDK C2012X5R0J106MT

Over Voltage Protection (OVP)

The NCP5030 regulates the load current. If there is an open load condition such as a lost connection to the White LED, the converter keeps supplying current to the Cout capacitor causing the output voltage to rise rapidly. To prevent the device from being damaged and to eliminate external protection components such as zener diode, the NCP5030 incorporates an OVP circuit, which monitors the output voltage with a resistive divider network and a comparator and voltage reference. If the output reaches 6 V (nominal), the OVP circuit will detect a fault and inhibit PWM operation. This comparator has 200 mV hysteresis to allow the PWM operation to resume automatically when the load is reconnected and when the voltage drops below 5.8 V.

Under Voltage Lock Out

To ensure proper operation under low input voltage conditions, the device has a built−in Under−Voltage Lock Out (UVLO) circuit. The device remains disabled until the input voltage exceeds 2.35 V (nominal). This circuit has 100 mV hysteresis to provide noise immunity to transient conditions.

Thermal Protection

Normal operation of the NCP5030 is disabled to protect the device if the junction temperature exceeds 160°C. When the junction temperature drops below 140°C, normal operation will resume.

Layout Recommendations

As with all switching DC/DC converter, care must be observed to the PCB board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device any copper trace, which see high frequency switching path, should be optimized. So the input and output bypass ceramic capacitor, C_{IN} and C_{OUT} as depicted in Figure 24 must be placed as close as possible the NCP5030 and connected directly between pins and ground plane. In additional, the track connection between the inductor and the switching input, SW pin must be minimized to reduce EMI radiation.

TBD

Figure 24. Recommended PCB Layout

ORDERING INFORMATION

Device	Package	Shipping †
NCP5030MTTXG	WDFN12, 3x4 mm (Pb−Free)	3000/Tape & Reel

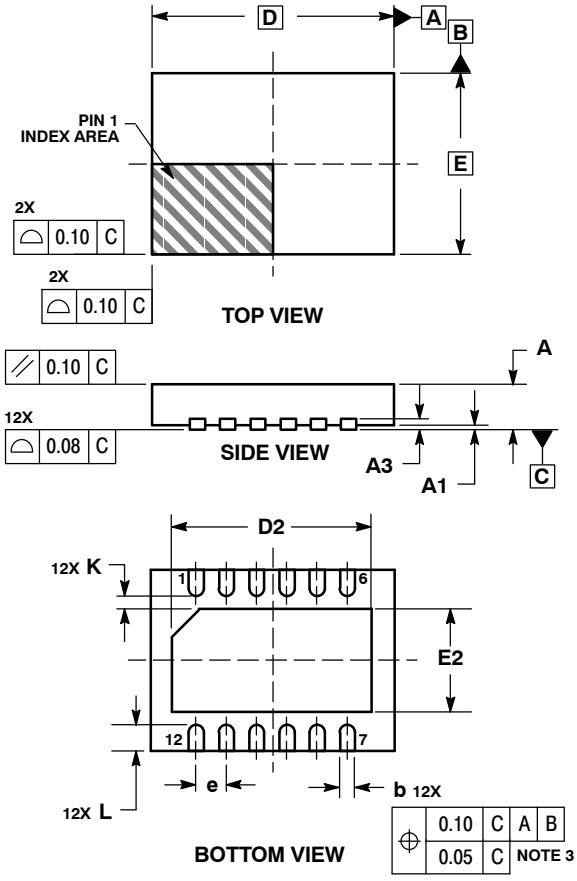
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Demo Board Available:

The NCP5030MTTXGEVB/D evaluation board that configures the device to drive high current through one white LED.

PACKAGE DIMENSIONS

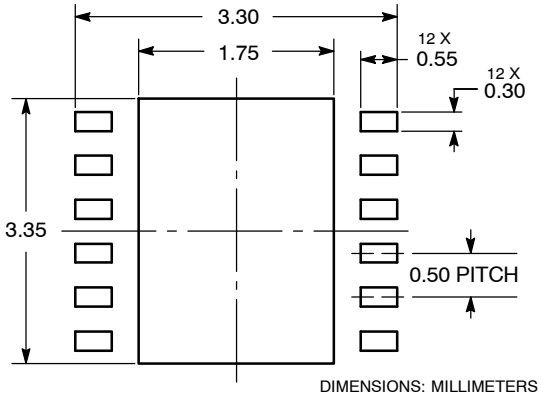
WDFN12, 3x4, 0.5P
CASE 506AY−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	3.20	3.40
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Literature Distribution Center for ON Semiconductor
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