USBP01-5M8

ESD protection for enhanced micro USB interface

Datasheet – production data

Features

- D+/D- and ID lines protection with 7 V low voltage diodes (LV)
- V_{BUS} line protection with 32 V high voltage diodes (HV)
- Ultra low capacitance 0.2 pF on low voltage diodes
- 10 GHz bandwidth at -3 dB
- 1.35 mm width and 0.4 mm height package
- RoHS compliant

Complies with following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

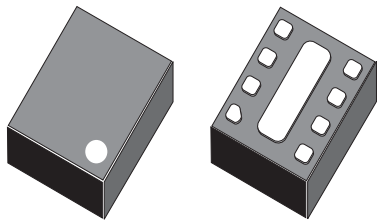
Where transient over-voltage protection in ESD sensitive equipment is required for enhanced micro USB, such as:

- Cellular phone handsets and accessories
- Portable multimedia players and accessories
- Notebooks
- Digital cameras and camcorders
- Communication systems

Description

The USBP01-5M8 is an application specific discrete device dedicated to ESD protection of an enhanced mini / micro USB interface able to manage USB, audio, TV out and FM signals.

The device is ideal for applications where both reduced printed circuit board space and low power absorption capability are required.



µQFN-8L package

Figure 1. Pin configuration (top view)

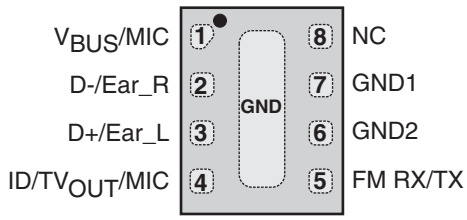
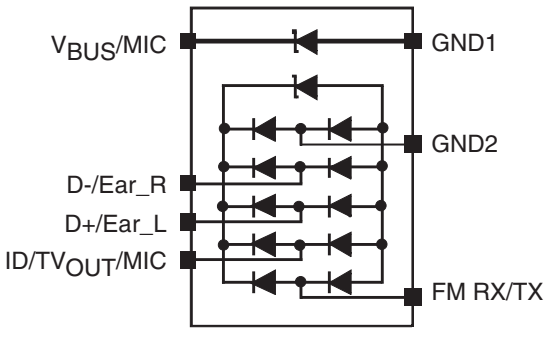


Figure 2. Functional diagram



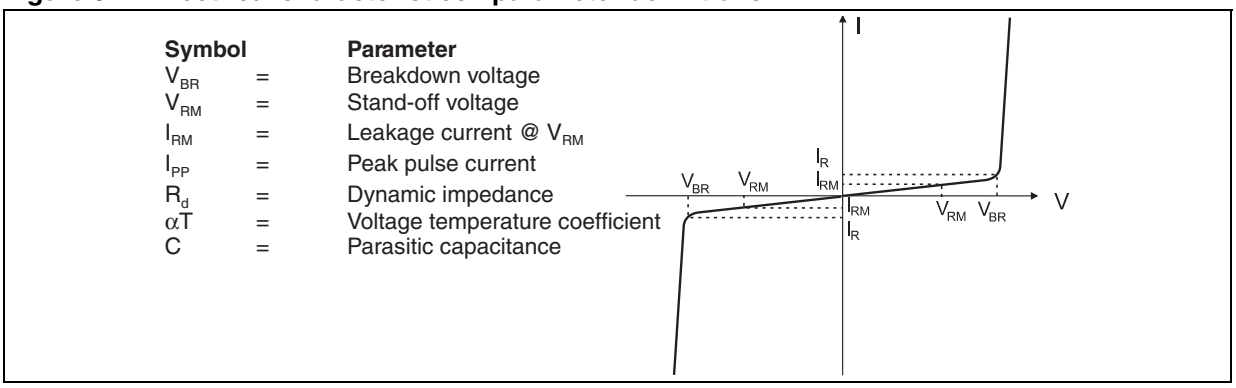
1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter		Value	Unit
V_{PP_VBUS}	Peak pulse voltage on pin 1 (V_{BUS} - GND1)	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	30 30	kV
V_{PP_Data}	Peak pulse voltage between pins 2 to 5 and GND2	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	8 15	kV
P_{PP_VBUS}	Peak pulse power (8/20 µs) - pin V_{BUS} to pin GND1 (1) Peak pulse power (8/20 µs) - pin GND1 to pin V_{BUS} (1)		200 90	W
I_{PP_VBUS}	Peak pulse current (8/20 µs) on V_{BUS}		6	A
T_j	Operating junction temperature range		-55 to + 150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 3. Electrical characteristics - parameter definitions



1.1 V_{BUS} pin (pin 1)

Table 2. Electrical characteristics T_{amb} = 25 °C, otherwise specified

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA - pin V_{BUS} to pin GND1	32	35		V
	I_R = 1 mA - pin GND1 to pin V_{BUS}	14	16		
I_{RM}	V_{RM} = 28 V - pin V_{BUS} to pin GND1		30	100	nA
	V_{RM} = 12.5 - pin GND1 to pin V_{BUS}		30	100	
C_{line}	F = 1 MHz, V_R = 0 V		30	40	pF
V_{CL}	I_{PP} = 1 A - pin V_{BUS} to pin GND1			40	V
	I_{PP} = 1 A - pin GND1 to pin V_{BUS}			20	

Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge on V_{BUS})

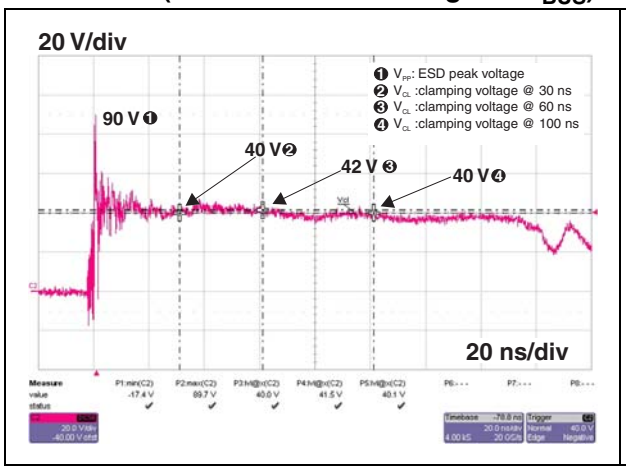


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge on V_{BUS})

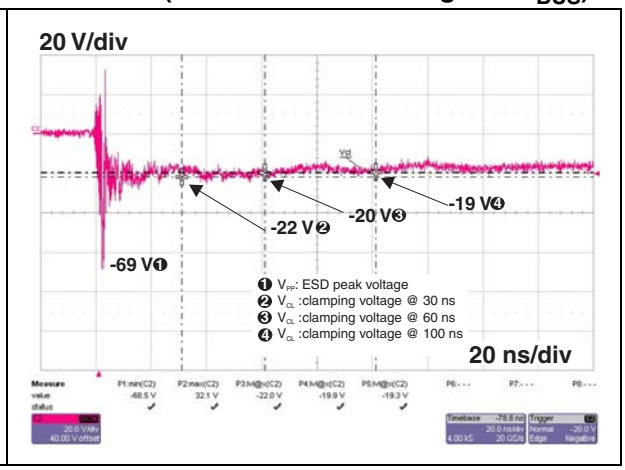


Figure 6. Peak pulse power versus initial junction temperature (maximum values)

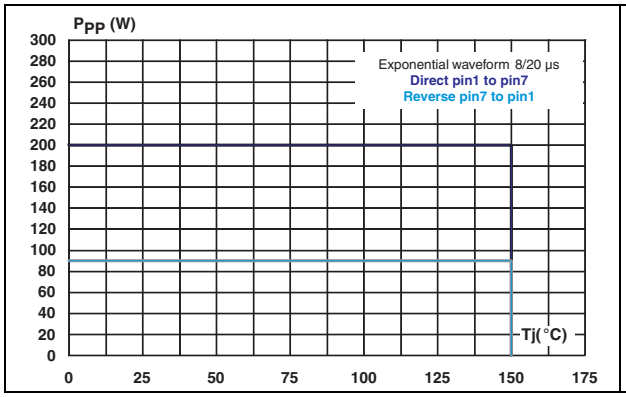
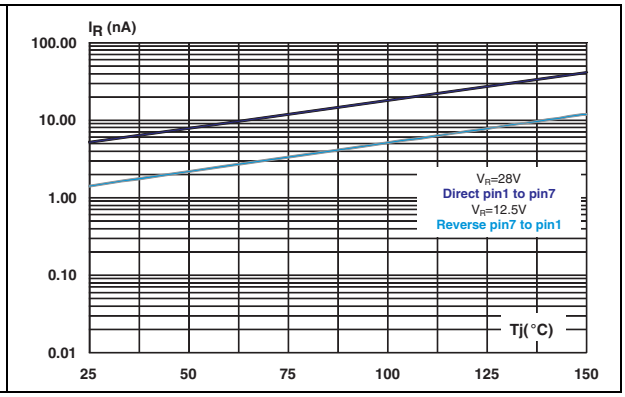


Figure 7. Leakage current versus junction temperature (typical values)



1.2 D/Ear (pin 2 and 3), FM Tx/Tx (pin5), ID/TV out/MIC (pin 4)

Table 3. Electrical characteristics T_{amb} = 25 °C, otherwise specified

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	9		V
I_{RM}	V_{RM} = 3 V			70	nA
BW	Bandwidth (-3 dB)		10		GHz
C_{line}	F = 200 to 3000 MHz, V_R = 0 V		0.2	0.3	pF

Figure 8. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

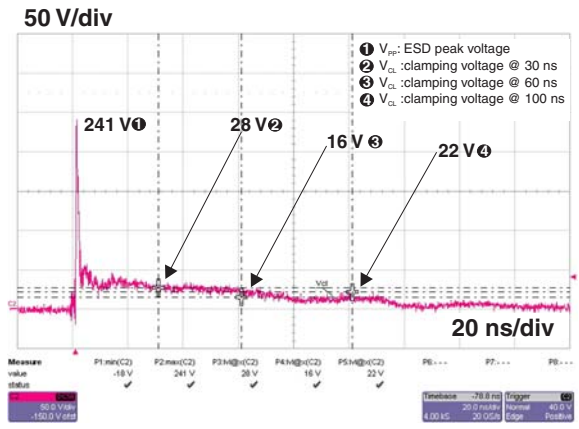


Figure 9. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

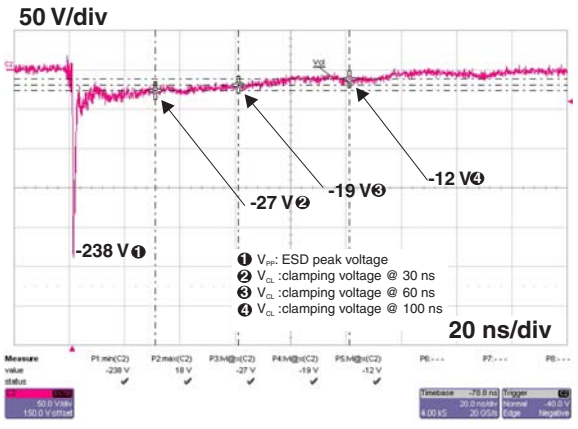


Figure 10. S21 attenuation measurement

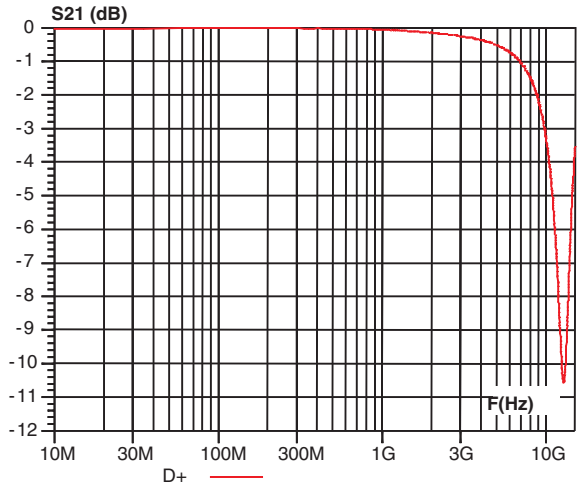


Figure 11. Junction capacitance versus reverse applied voltage (typical values)

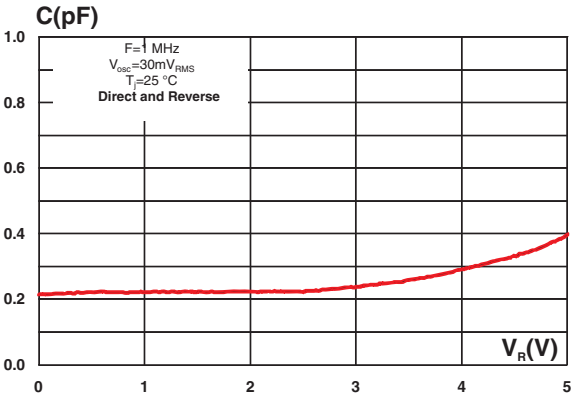


Figure 12. Eye diagram PCB only

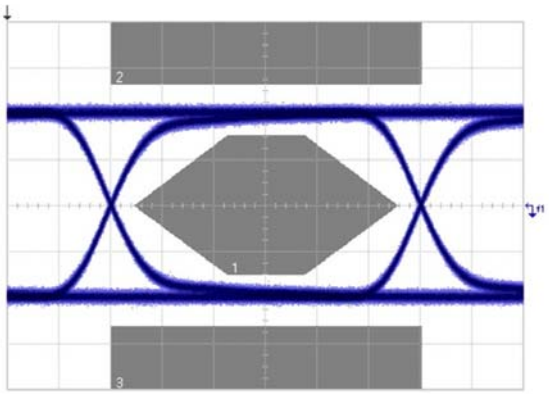
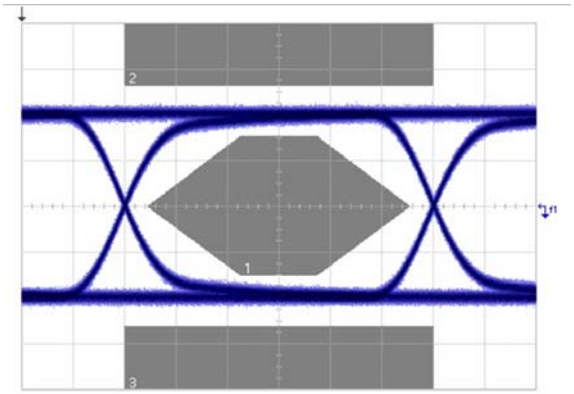
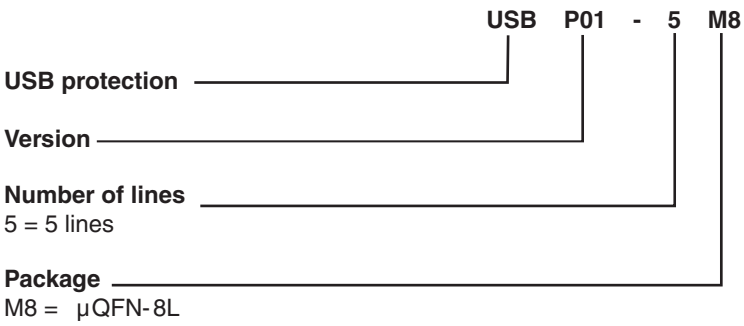


Figure 13. Eye diagram PCB + USBP01-5M8



2 Ordering information scheme

Figure 14. Ordering information scheme

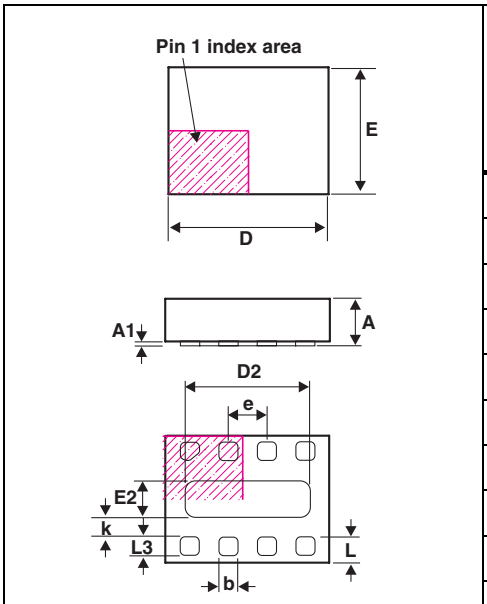


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 4. µQFN-8L dimensions



Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.31	0.38	0.40	0.012	0.015	0.016
A1	0.00	0.02	0.05	0.00	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.60	1.7	1.80	0.063	0.067	0.071
D2	1.15	1.30	1.40	0.045	0.051	0.055
E	1.25	1.35	1.45	0.049	0.053	0.057
E2	0.25	0.40	0.50	0.010	0.016	0.020
e	0.35	0.40	0.45	0.014	0.016	0.018
k	0.15	0.23	0.30	0.006	0.009	0.012
L	0.175	0.25	0.325	0.007	0.010	0.013
L3	0.15	0.20	0.25	0.006	0.008	0.010

Figure 15. Foot print recommendations (dimensions in mm)

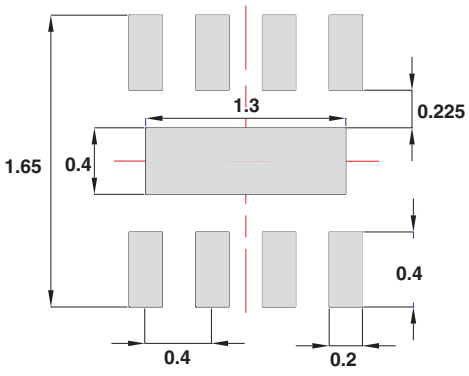


Figure 16. Marking

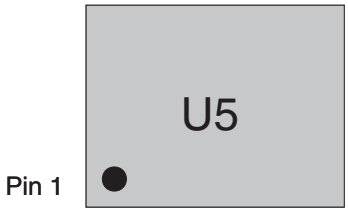
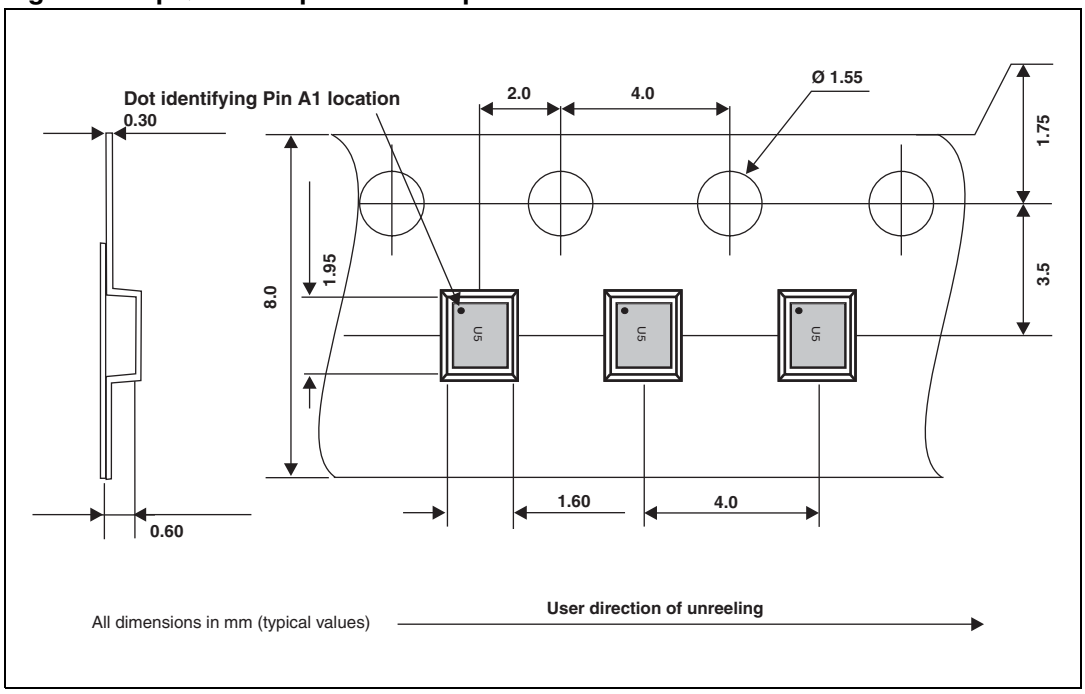


Figure 17. µQFN-8L tape and reel specifications



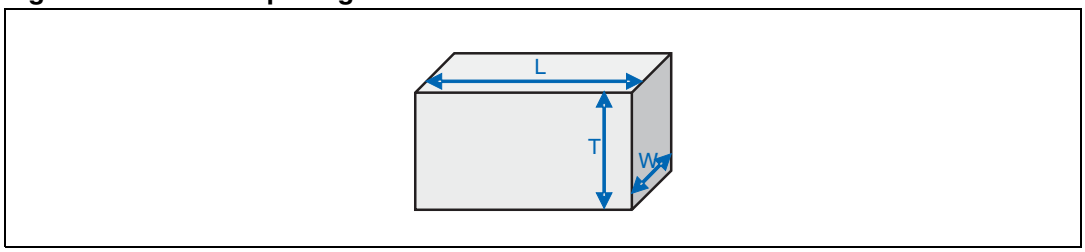
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 18. Stencil opening dimensions



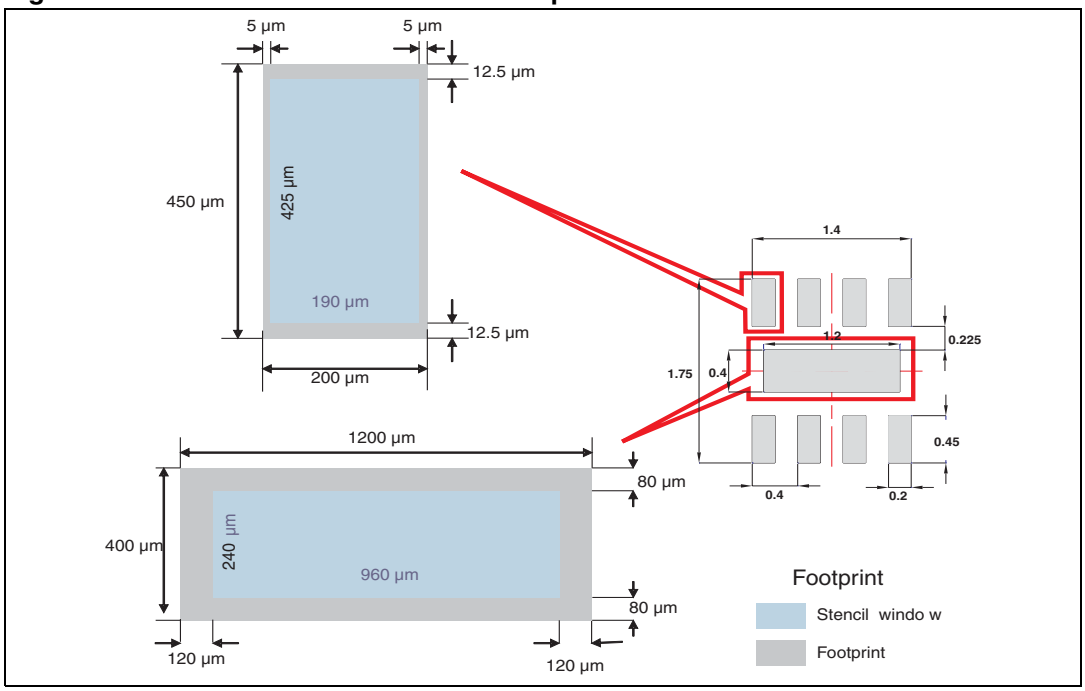
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 19. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

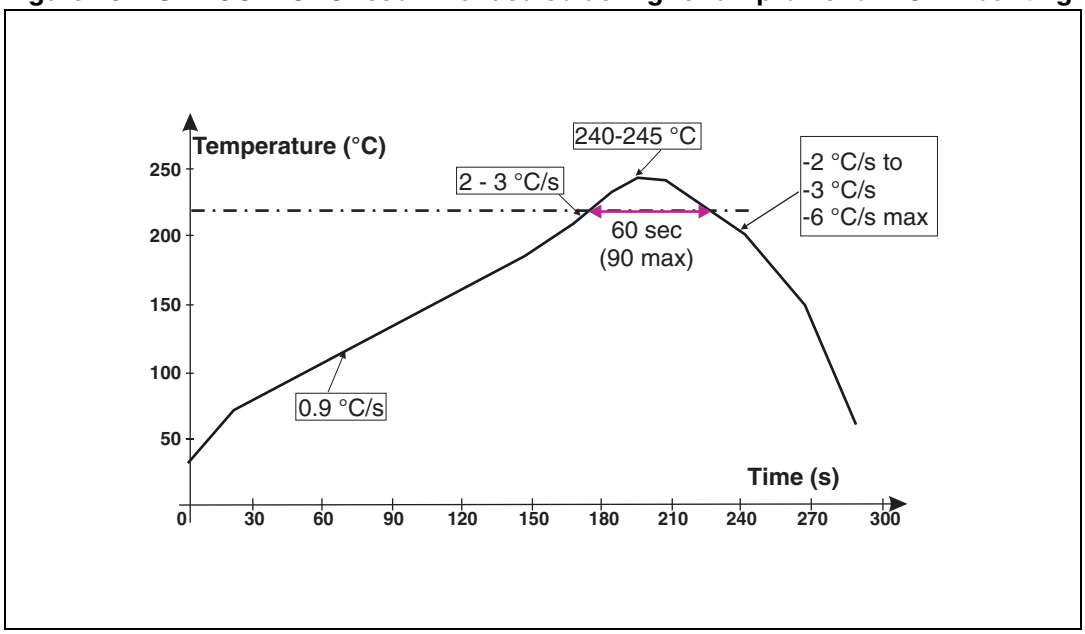
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 20. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBP01-5M8	U5(1)	µQFN-8L	2.17 mg	400	Tape and reel (7”)

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
08-Jun-2012	1	Initial release.

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