NB6L16

2.5V / 3.3V Multilevel Input to Differential LVPECL/LVNECL Clock or Data Receiver/ Driver/Translator Buffer

The NB6L16 is a high precision, low power ECL differential clock or data receiver/driver/translator buffer. The device is functionally equivalent to the EL16, EP16, LVEL16 and NBSG16 devices. With output transition times of 70 ps, it is ideally suited for high frequency, low power systems. The device is targeted for Backplane buffering, GbE clock/data distribution, Fibre Channel distribution and SONET clock/data distribution applications.

Input accept LVNECL (Negative ECL), LVPECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are 800 mV ECL signals.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- Input Clock Frequency ≥ 6 GHz
- Input Data Rate Frequency ≥ 6 Gb/s
- Low 12 mA Typical Power Supply Current
- 70 ps Typical Rise/Fall Times
- 130 ps Input Propagation Delay
- On−Chip Reference for ECL Single−Ended Input − V_{BB} Output
- PECL Mode Operating Range:
  V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- Open Input Default State
- LVDS, LVPECL, LVNECL, LVCMOS, LVTTL and CML Input Compatible
- Pb−Free Packages are Available

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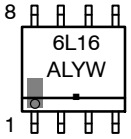
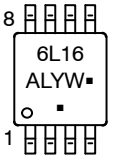
MARKING DIAGRAMS*

SOIC−8
D SUFFIX
CASE 751



TSSOP−8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

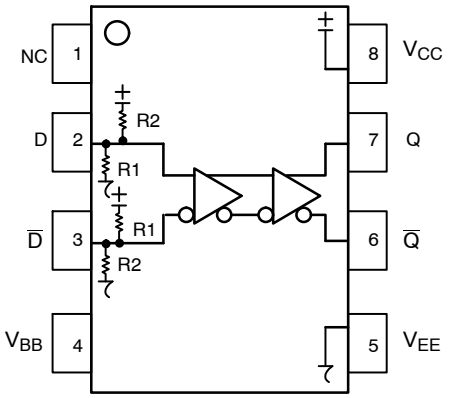


Figure 1. Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Default State	Description
1	NC	–	–	No Connect. The NC pin is electrically connected to the die and MUST be left open.
2	D	LVDS, CML, LVPECL, LVNECL, LVTTL, LVCMOS Input	LOW	Non−inverted differential clock/data input. Internal 75 kΩ to V_{CC} and 37.5 kΩ to V_{EE}.
3	$\overline{D}$	LVDS, CML, LVPECL, LVNECL, LVTTL, LVCMOS Input	HIGH	Inverted differential clock/data input. Internal 37.5 kΩ to V_{CC} and 75 kΩ to V_{EE}.
4	V_{BB}	–	–	Internally generated ECL reference voltage supply.
5	V_{EE}	–	–	Negative power supply voltage.
6	$\overline{Q}$	ECL Output		Inverted differential ECL output. Typically terminated with 50 Ω resistor to V_{CC} − 2.0 V.
7	Q	ECL Output		Non−inverted differential ECL output. Typically terminated with 50 Ω resistor to V_{CC} − 2.0 V.
8	V_{CC}	–	–	Positive power supply voltage.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Default State Resistor	(R1)	37.5 kΩ
Internal Input Default State Resistor	(R2)	75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 1 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 1.125 in
Transistor Count		167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–3.6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 –3.6	V V
I_{out}	Output Current	Continuous Surge		25 50	mA mA
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	SOIC–8 SOIC–8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	Standard Board	SOIC–8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	TSSOP–8 TSSOP–8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	Standard Board	TSSOP–8	41 to 44	°C/W
T_{sol}	Wave Solder Standard Pb–Free	≤ 3 sec @ 248°C ≤ 3 sec @ 260°C		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 4)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current (Note 5)	10	12	18	10	12	18	10	12	18	mA
V_{OH}	Output HIGH Voltage (Note 6)	1350	1450	1550	1400	1500	1600	1450	1550	1650	mV
V_{OL}	Output LOW Voltage (Note 6)	565	725	870	630	765	920	690	825	970	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 10, 12) (Note 8)											
V_{th}	Input Threshold Reference Voltage Range (Notes 2, 7)	1125		V_{CC} −75	1125		V_{CC} −75	1125		V_{CC} −75	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} +75		V_{CC}	V_{th} +75		V_{CC}	V_{th} +75		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	V_{EE}		V_{th} −75	V_{EE}		V_{th} −75	V_{EE}		V_{th} −75	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 11, 13) (Note 9)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} −75	V_{EE}		V_{CC} −75	V_{EE}		V_{CC} −75	mV
V_{CMR}	Input Common Mode Range (Differential Cross−Point Voltage) (Note 3)	950		V_{CC} −38	950		V_{CC} −38	950		V_{CC} −38	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2500	75		2500	75		2500	mV
I_{IH}	Input HIGH Current D $\overline{D}$		50 10	150 150		50 10	150 150		50 10	150 150	μA
I_{IL}	Input LOW Current D $\overline{D}$	−150 −150	−5 −30		−150 −150	−5 −30		−150 −150	−5 −30		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. V_{th} is applied to the complementary input when operating in single−ended mode.
3. V_{CMR} minimum varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to −1.3 V.
5. All input and output pins left open.
6. All loading with 50 Ω to V_{CC} − 2.0 V.
7. Do not use V_{BB} as a reference voltage for single−ended PECL signals when operating device at V_{CC} − V_{EE} < 3.0 V.
8. V_{th}, V_{IH}, and V_{IL} parameters must be complied with simultaneously.
9. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 5. DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 12)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 13)	10	12	18	10	12	18	10	12	18	mA
V_{OH}	Output HIGH Voltage (Note 14)	2150	2250	2350	2200	2300	2400	2250	2350	2450	mV
V_{OL}	Output LOW Voltage (Note 14)	1365	1525	1670	1430	1565	1720	1490	1625	1770	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 10, 12) (Note 15)											
V_{th}	Input Threshold Reference Voltage Range (Note 10)	1125		V_{CC} −75	1125		V_{CC} −75	1125		V_{CC} −75	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} +75		V_{CC}	V_{th} +75		V_{CC}	V_{th} +75		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	V_{EE}		V_{th} −75	V_{EE}		V_{th} −75	V_{EE}		V_{th} −75	mV
V_{BB}	Output Voltage Reference	1880	1980	2070	1880	1980	2070	1880	1980	2070	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 11, 13) (Note 16)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} −75	V_{EE}		V_{CC} −75	V_{EE}		V_{CC} −75	mV
V_{CMR}	Input Common Mode Range (Differential Cross−Point Voltage) (Note 11)	950		V_{CC} −38	950		V_{CC} −38	950		V_{CC} −38	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2500	75		2500	75		2500	mV
I_{IH}	Input HIGH Current D $\overline{D}$		50 10	150 150		50 10	150 150		50 10	150 150	μA
I_{IL}	Input LOW Current D $\overline{D}$	−150 −150	−5 −30		−150 −150	−5 −30		−150 −150	−5 −30		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. V_{th} is applied to the complementary input when operating in single−ended mode.
11. V_{CMR} minimum varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to −0.5 V.
13. All input and output pins left open.
14. All loading with 50 Ω to V_{CC} − 2.0 V.
15. V_{th}, V_{IH}, and V_{IL} parameters must be complied with simultaneously.
16. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 6. DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −3.465 V to −2.375 V (Note 19)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 21)	10	12	18	10	12	18	10	12	18	mA
V_{OH}	Output HIGH Voltage (Note 20)	−1150	−1050	−950	−1100	−1000	−900	−1050	−950	−850	mV
V_{OL}	Output LOW Voltage (Note 20)	−1935	−1775	−1630	−1870	−1735	−1580	−1810	−1675	−1530	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 10, 12) (Note 22)											
V_{th}	Input Threshold Reference Voltage Range (Note 10)	V_{EE} +1125		V_{CC} −75	V_{EE} +1125		V_{CC} −75	V_{EE} +1125		V_{CC} −75	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} +75		V_{CC}	V_{th} +75		V_{CC}	V_{th} +75		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	V_{EE}		V_{th} −75	V_{EE}		V_{th} −75	V_{EE}		V_{th} −75	mV
V_{BB}	Output Voltage Reference	−1420	−1320	−1230	−1420	−1320	−1230	−1420	−1320	−1230	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 11, 13) (Note 23)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE}+ 1200		V_{CC}	V_{EE}+ 1200		V_{CC}	V_{EE}+ 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} −75	V_{EE}		V_{CC} −75	V_{EE}		V_{CC} −75	mV
V_{CMR}	Input Common Mode Range (Differential Cross−Point Voltage) (Note 11)	V_{EE}+ 950		V_{CC} −38	V_{EE}+ 950		V_{CC} −38	V_{EE}+ 950		V_{CC} −38	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2500	75		2500	75		2500	mV
I_{IH}	Input HIGH Current D D		50 10	150 150		50 10	150 150		50 10	150 150	μA
I_{IL}	Input LOW Current D D	−150 −150	−5 −30		−150 −150	−5 −30		−150 −150	−5 −30		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. V_{th} is applied to the complementary input when operating in single−ended mode.
18. V_{CMR} minimum varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}.
19. Input and output parameters vary 1:1 with V_{CC}.
20. All loading with 50 Ω to V_{CC} − 2.0 V.
21. All input and output pins left open.
22. V_{th}, V_{IH}, and V_{IL} parameters must be complied with simultaneously.
23. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 7. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V (Note 24)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OUTPP}	Output Voltage Amplitude f_{in} < 3 GHz (See Figures 2 & 3) f_{in} < 6 GHz	 500 270	 700 350		 500 270	 700 350		 500 270	 700 300		mV
f_{DATA}	Maximum Operating Data Rate	6									Gb/s
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential @ 1 GHz	80	130	180	80	130	180	85	135	185	ps
t_{SKEW}	Duty Cycle Skew (Note 25) Device−to−Device Skew		3 30	25 60		3 30	25 60		3 30	25 60	ps
t_{JITTER}	RMS Random Clock Jitter (Note 26) f_{in} < 6 GHz Peak−to−Peak Data Dependent JItter (Note 27) f_{in} < 6 Gb/s		 0.2 2	 1 12		 0.2 2	 1 12		 0.2 2	 1 12	ps
V_{INPP}	Input Voltage Swing / Sensitivity (Differential Configuration) (Note 28)	75	700	2500	75	700	2500	75	700	2500	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%)	30	70	120	30	70	120	30	70	120	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

24. Measured using a 800 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
25. See Figure 9 $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. Skew is measured between outputs under identical transitions and conditions @ 1 GHz.
26. Additive RMS jitter with 50% duty cycle clock signal at 6 GHz.
27. Additive Peak−to−Peak data dependent jitter with NRZ PRBS 2^{23}−1 data rate at 6 Gb/s.
28. $V_{INPP(max)}$ cannot exceed $V_{CC} - V_{EE}$. (Applicable only when $V_{CC} - V_{EE}$ < 2500 mV). Input voltage swing is a single−ended measurement operating in the differential mode.

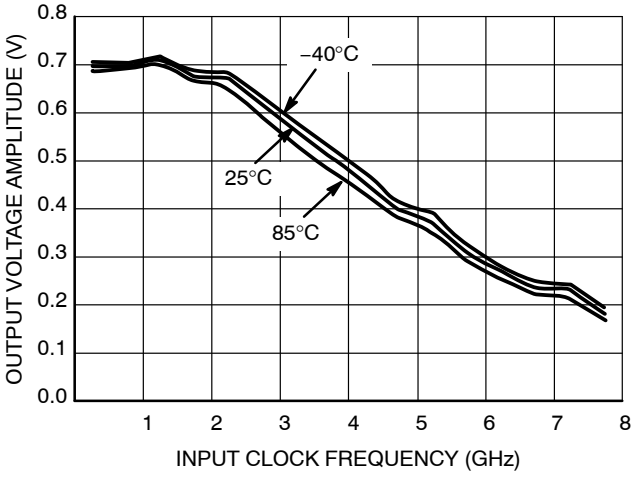


Figure 2. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{IN}) and Temperature at $V_{CC} - V_{EE}$ = 3.3 V

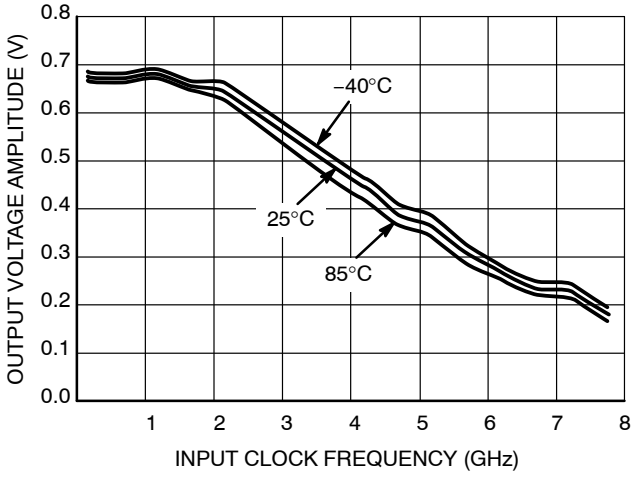


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{IN}) and Temperature at $V_{CC} - V_{EE}$ = 2.5 V

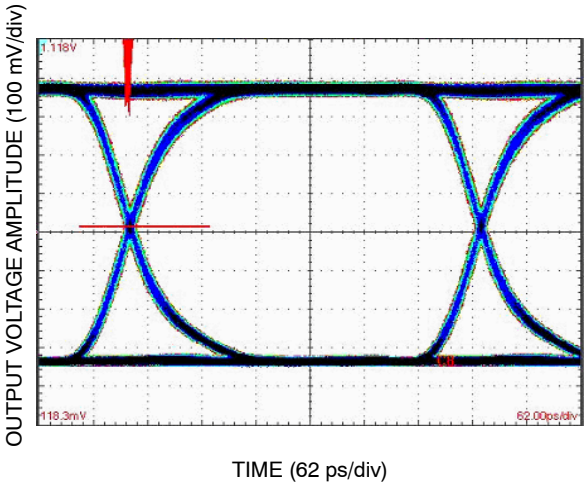


Figure 4. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23}–1 (Total System Pk–Pk Jitter is 16 ps. Device Pk–Pk Jitter Contribution is 3 ps)

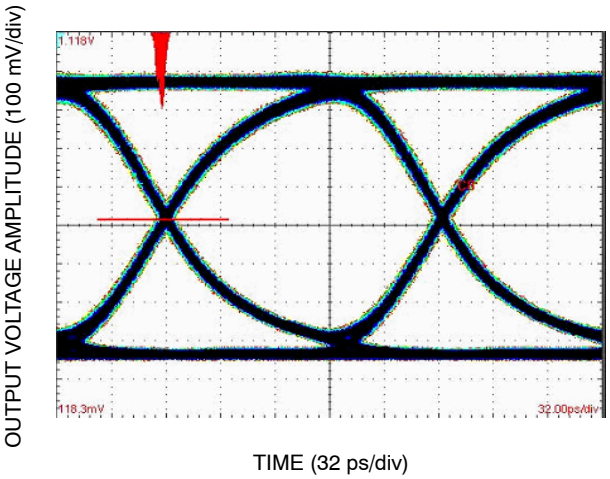


Figure 5. Typical Output Waveform at 6.125 Gb/s with PRBS 2^{23}–1 (Total System Pk–Pk Jitter is 17 ps. Device Pk–Pk Jitter Contribution is 4 ps)

NOTE: $V_{CC} - V_{EE}$ = 3.3 V; V_{IN} = 700 mV; T_A = 25°C.

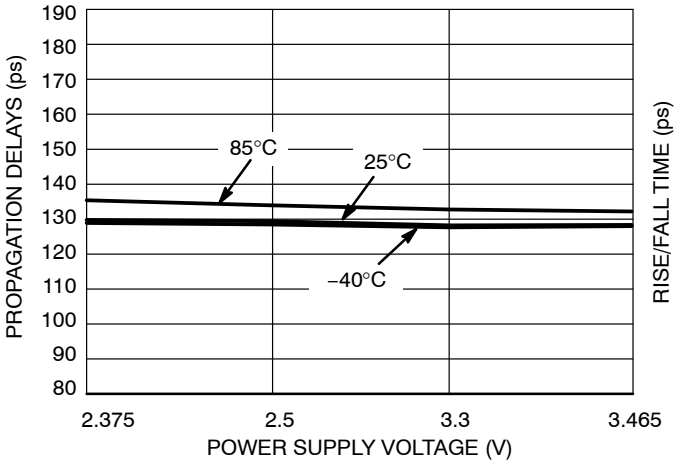


Figure 6. Propagation Delay versus Power Supply Voltage and Temperature

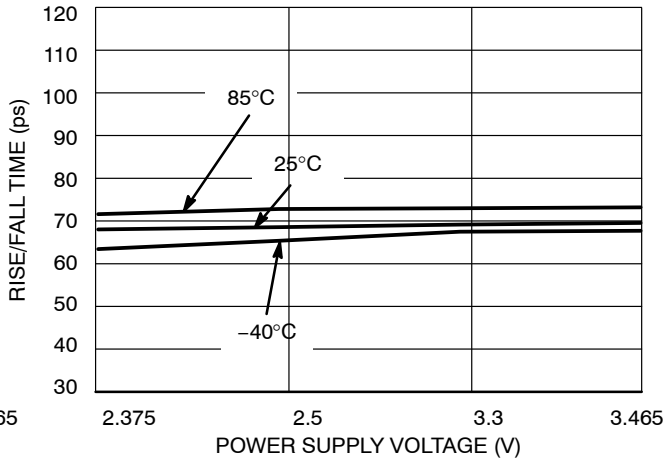


Figure 7. Rise/Fall Time versus Power Supply Voltage and Temperature

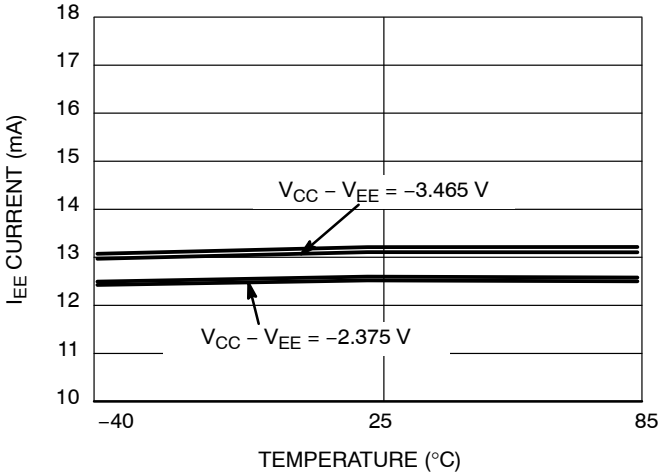


Figure 8. I_{EE} Current versus Temperature and Power Supply Voltage

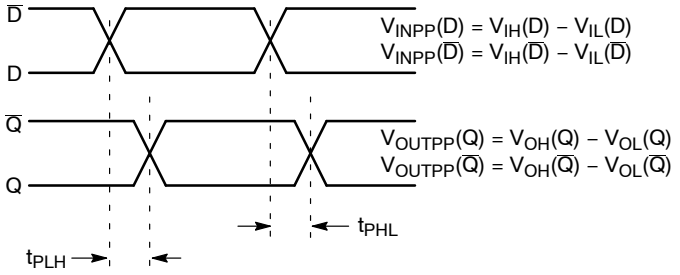


Figure 9. AC Reference Measurement

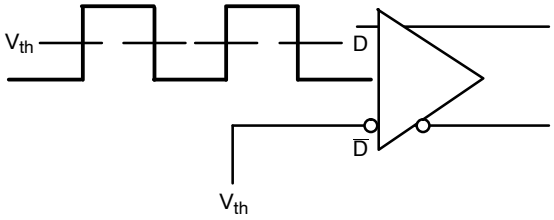


Figure 10. Differential Input Driven Single−Ended

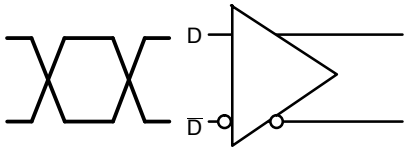


Figure 11. Differential Inputs Driven Differentially

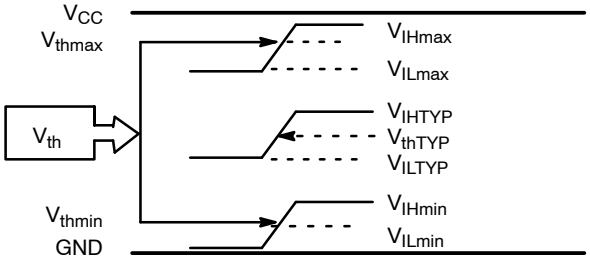


Figure 12. V_{th} Diagram

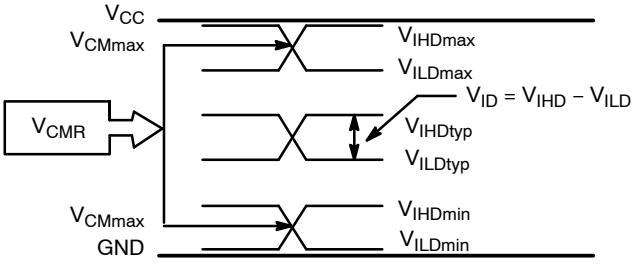


Figure 13. V_{CMR} Diagram

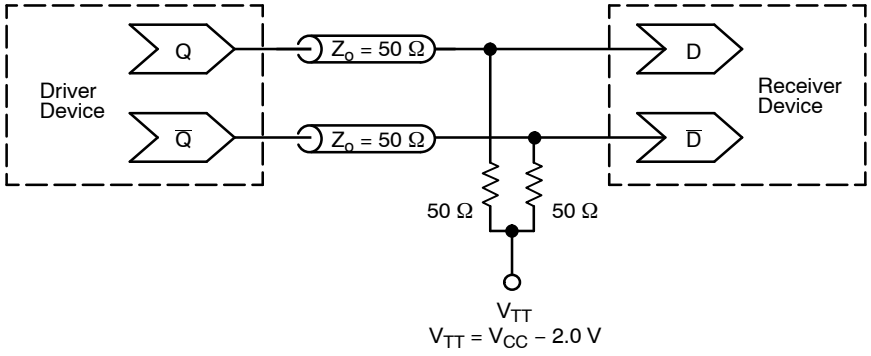


Figure 14. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
NB6L16D	SOIC−8	98 Units / Rail
NB6L16DG	SOIC−8 (Pb−Free)	98 Units / Rail
NB6L16DR2	SOIC−8	2500 / Tape & Reel
NB6L16DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NB6L16DT	TSSOP−8	100 Units / Rail
NB6L16DTG	TSSOP−8 (Pb−Free)	100 Units / Rail
NB6L16DTR2	TSSOP−8	2500 / Tape & Reel
NB6L16DTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

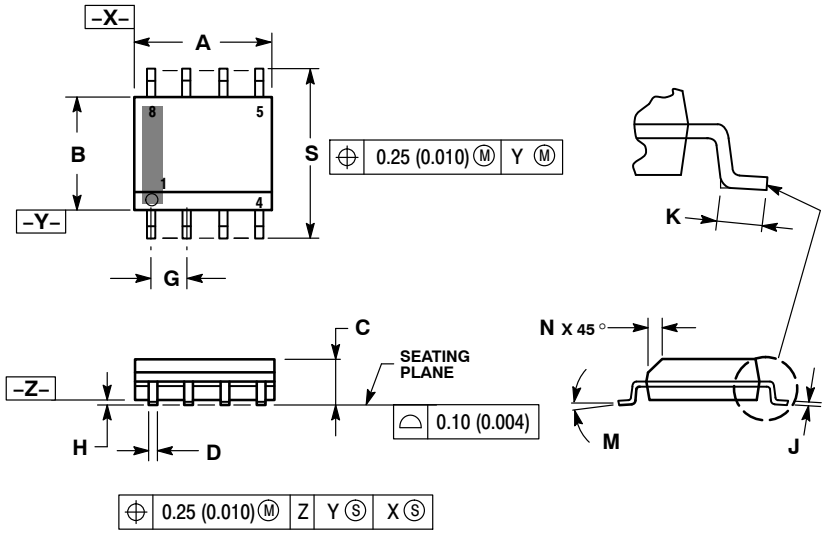
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

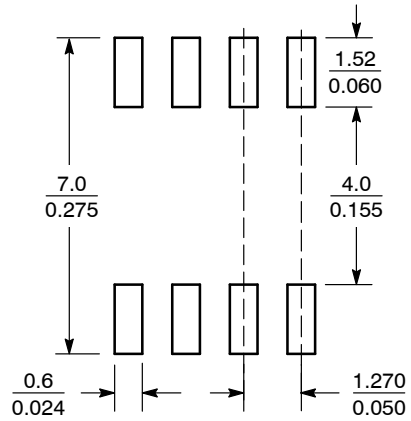
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

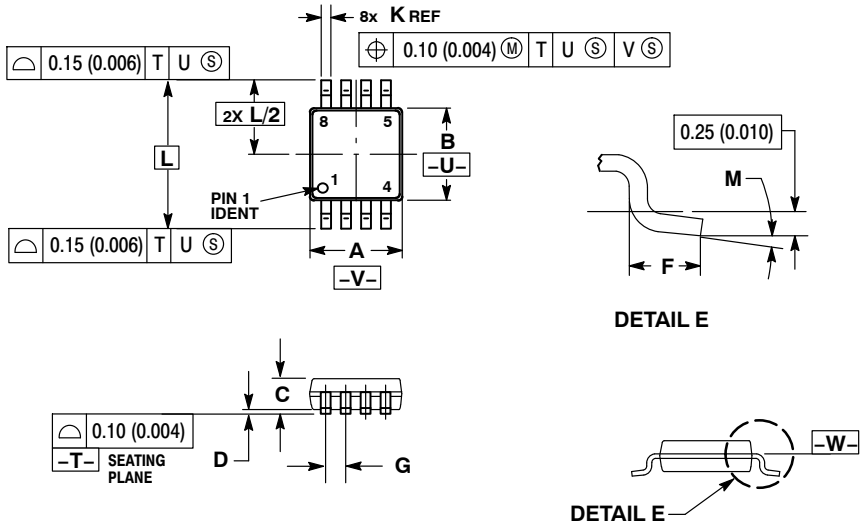


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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NB6L16/D