



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

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As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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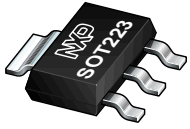
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Thank you for your cooperation and understanding,

WeEn Semiconductors





BT1308W-600D

4Q Triac

20 August 2013

Product data sheet

1. General description

Planar passivated four quadrant triac in a SOT223 surface-mountable plastic package. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- AC Fan controller
- General purpose low power phase control
- General purpose low power switching

4. Quick reference data

Table 1. Quick reference data

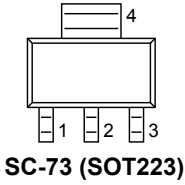
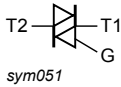
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|---|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 9 | A |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 107\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 0.8 | A |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 9 | - | 1 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 9 | - | 2 | 5 | mA |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|-----|-----|------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | 2 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | 4 | 7 | mA |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|---|---|
| 1 | T1 | main terminal 1 |  <p>SC-73 (SOT223)</p> |  <p>sym051</p> |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | T2 | main terminal 2 | | |

6. Ordering information

Table 3. Ordering information

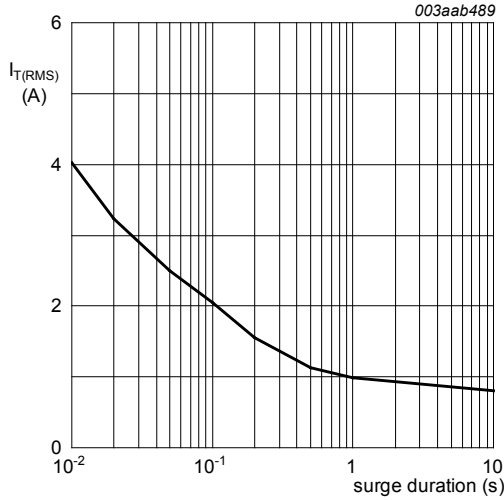
| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| BT1308W-600D | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|------|--------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 107\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 0.8 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 9 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 10 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.32 | A^2s |
| di_T/dt | rate of rise of on-state current | $I_T = 1\text{ A}$; $I_G = 20\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G+ | - | 50 | $A/\mu\text{s}$ |
| | | $I_T = 1\text{ A}$; $I_G = 20\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G- | - | 50 | $A/\mu\text{s}$ |
| | | $I_T = 1\text{ A}$; $I_G = 20\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2- G- | - | 50 | $A/\mu\text{s}$ |
| | | $I_T = 1\text{ A}$; $I_G = 20\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2- G+ | - | 10 | $A/\mu\text{s}$ |
| I_{GM} | peak gate current | | - | 1 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | $^{\circ}\text{C}$ |
| T_j | junction temperature | | - | 125 | $^{\circ}\text{C}$ |



f = 50 Hz; T_{sp} = 107 °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

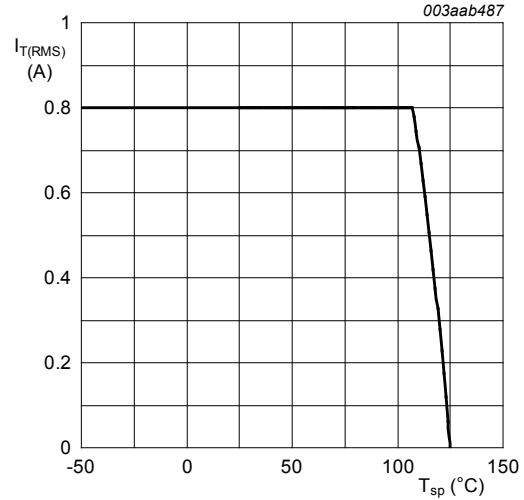
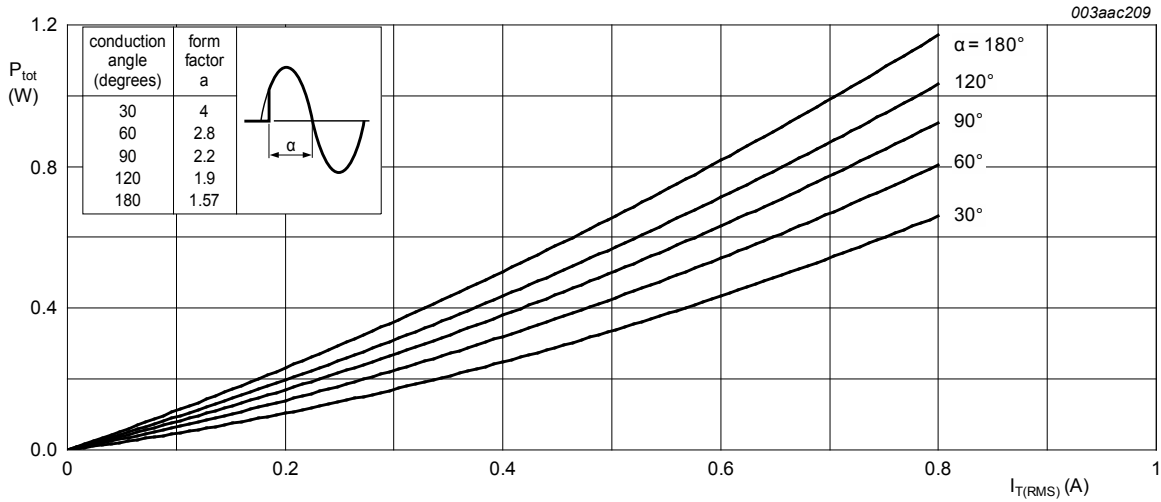


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

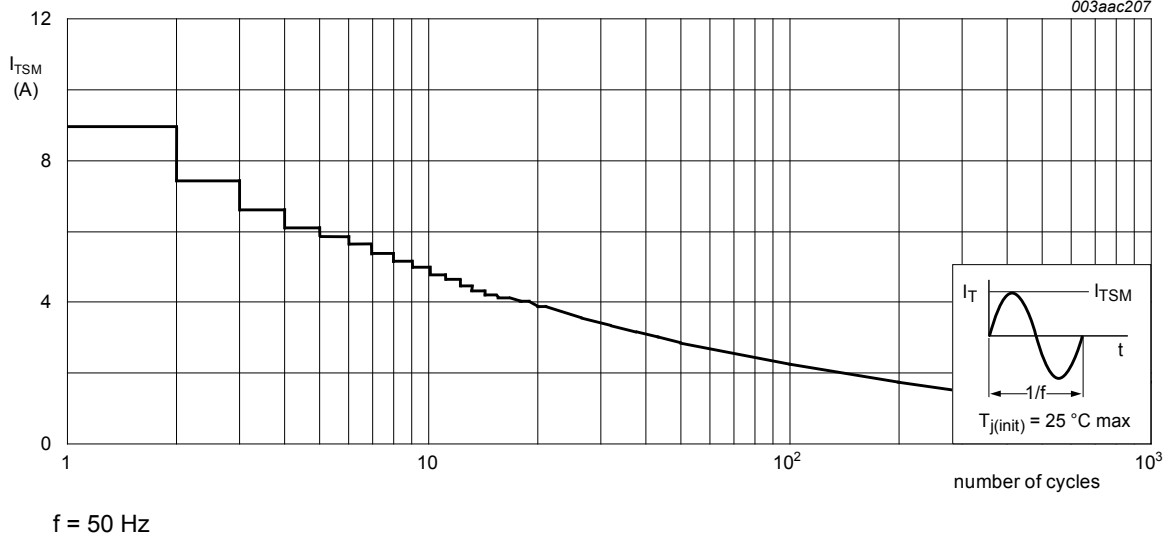


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

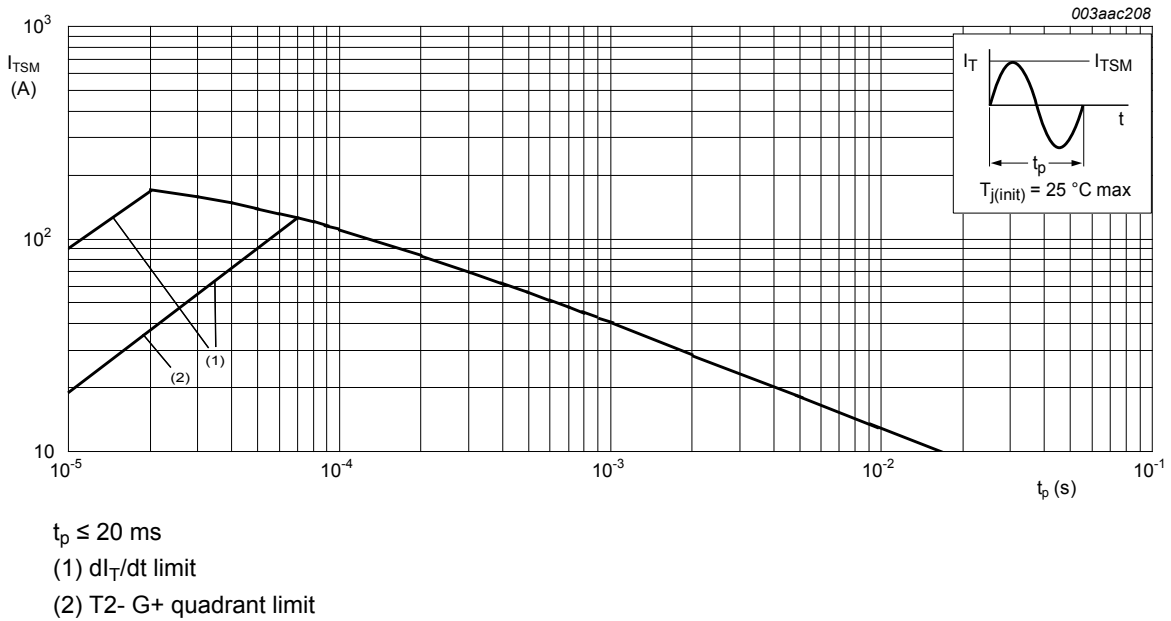
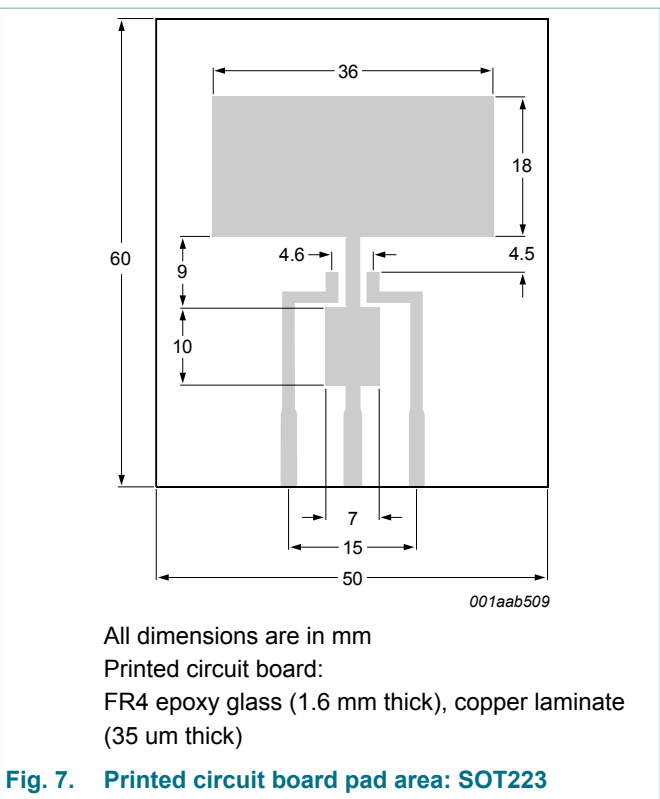
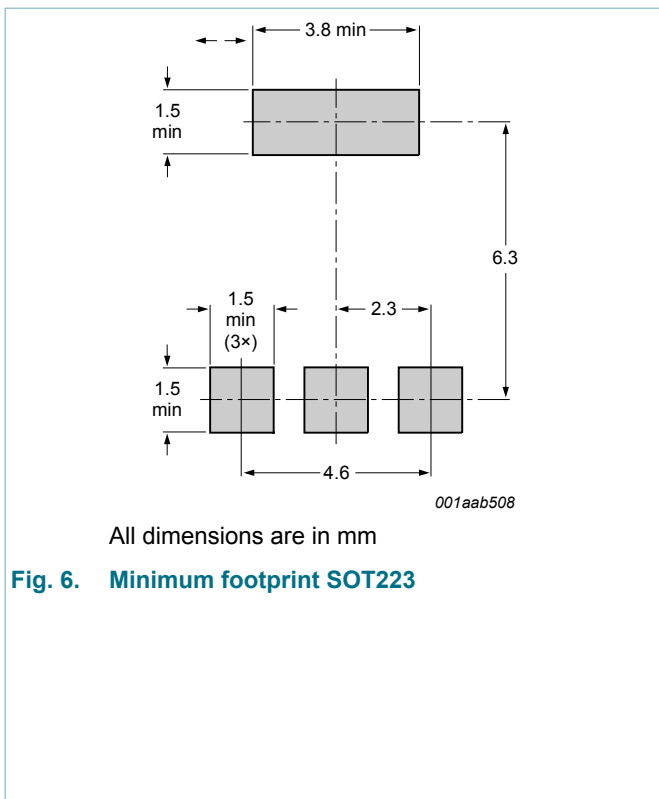


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|---|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle; Fig. 8 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | full cycle; for minimum footprint; Fig. 6 | - | 156 | - | K/W |
| | | full cycle; for pad area; Fig. 7 | - | 70 | - | K/W |



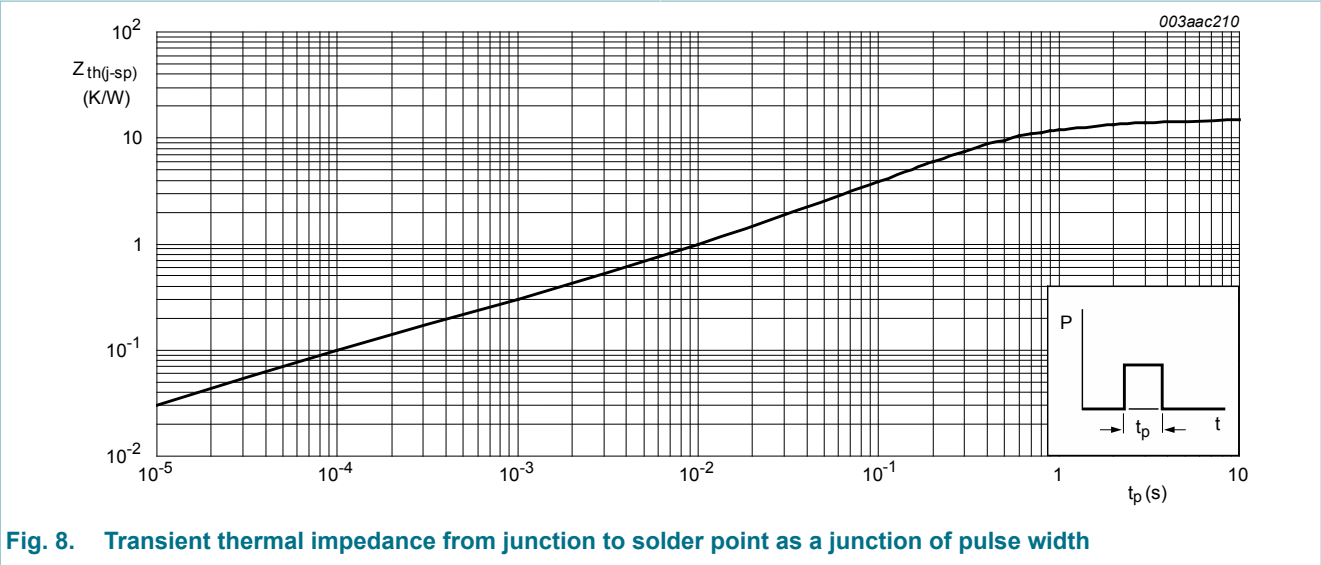
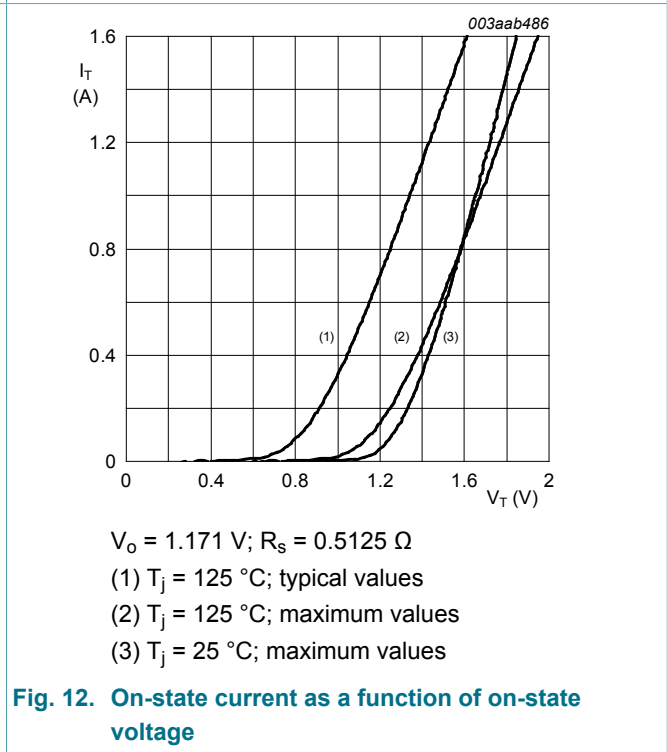
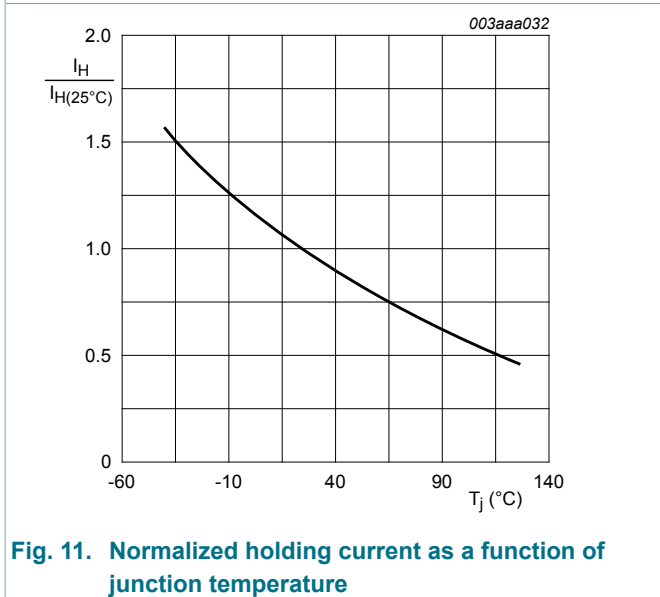
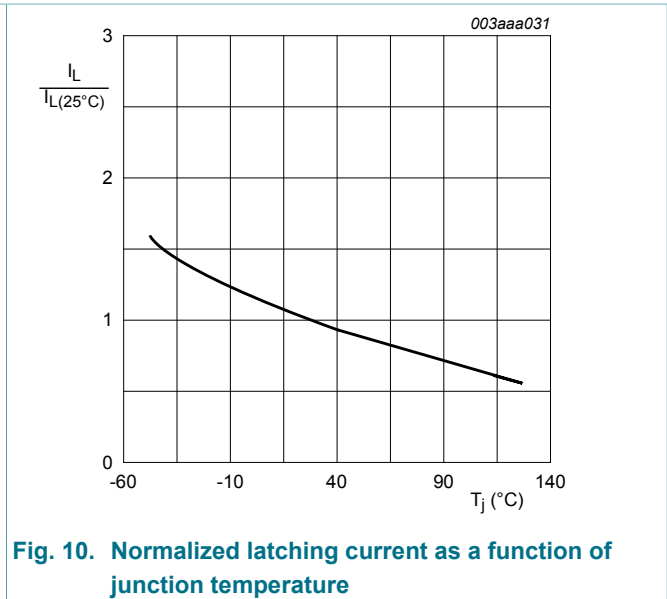
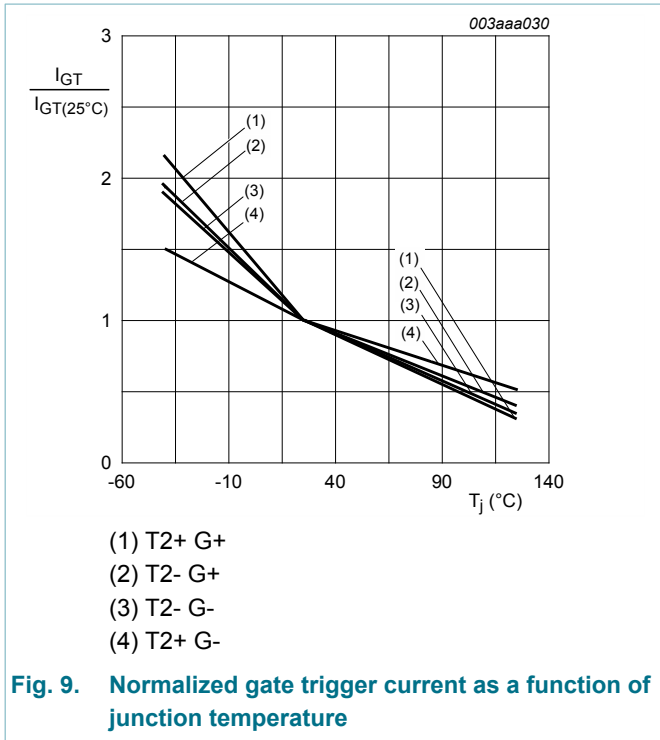


Fig. 8. Transient thermal impedance from junction to solder point as a junction of pulse width

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|---|-----|------|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | 1 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | 2 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | 2 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | 4 | 7 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1 | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 5 | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1 | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 2 | 10 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | 1 | 10 | mA |
| V_T | on-state voltage | $I_T = 0.85\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12 | - | 1.35 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13 | - | 0.9 | 1.5 | V |
| | | $V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 110\text{ }^\circ\text{C}$; Fig. 13 | 0.1 | 0.7 | - | V |
| I_D | off-state current | $V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$ | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 30 | 45 | - | V/ μs |
| dV_{com}/dt | rate of change of commutating voltage | $V_D = 600\text{ V}$; $T_j = 50\text{ }^\circ\text{C}$; $dI_{com}/dt = 0.3\text{ A/ms}$; $I_T = 0.84\text{ A}$; gate open circuit | - | 5 | - | V/ μs |
| t_{gt} | gate-controlled turn-on time | $I_{TM} = 1\text{ A}$; $V_D = 600\text{ V}$; $I_G = 25\text{ mA}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$ | - | 2 | - | μs |



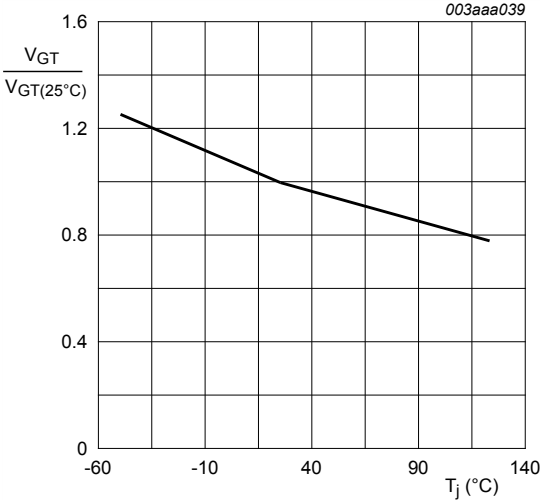


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

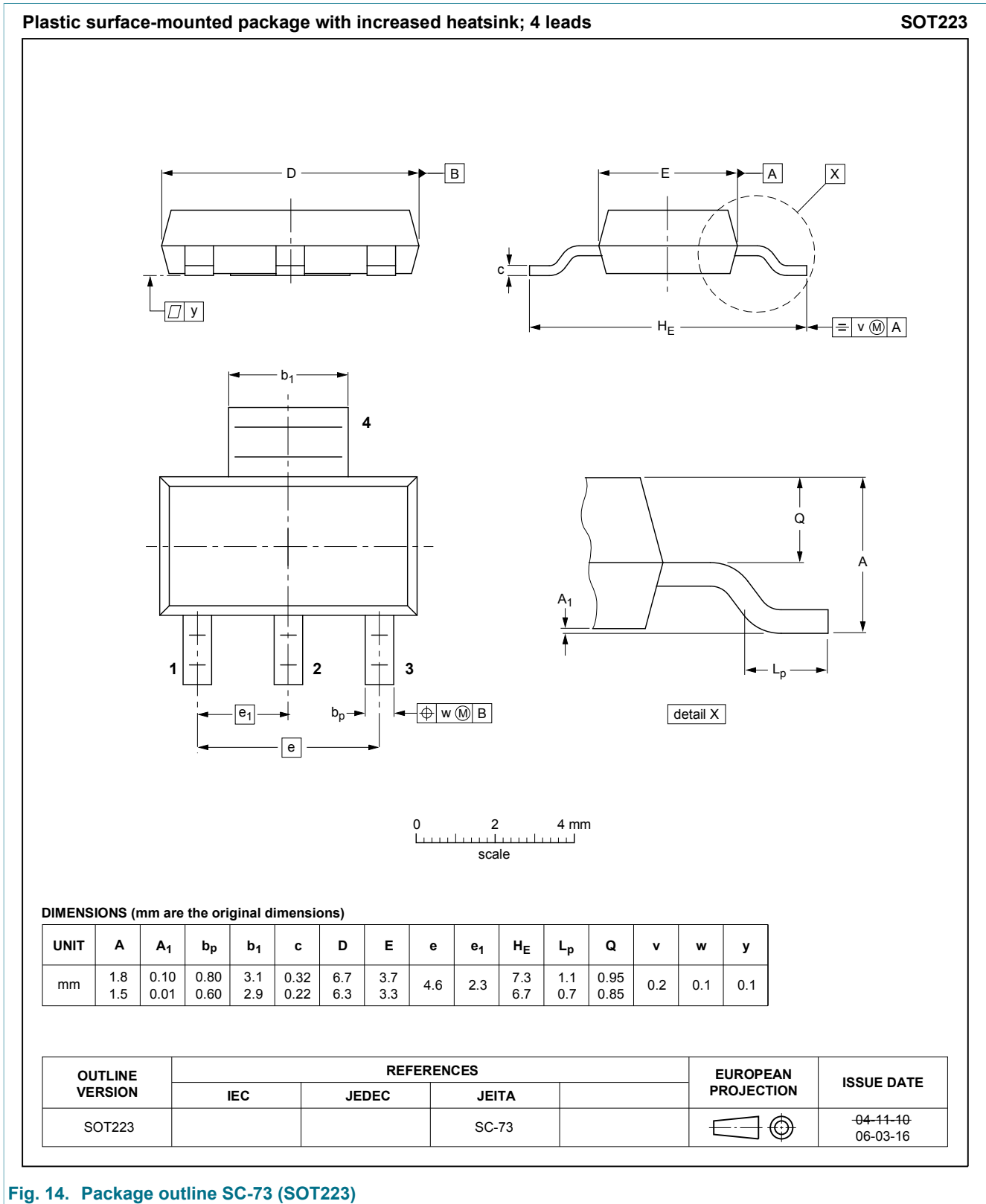


Fig. 14. Package outline SC-73 (SOT223)

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
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