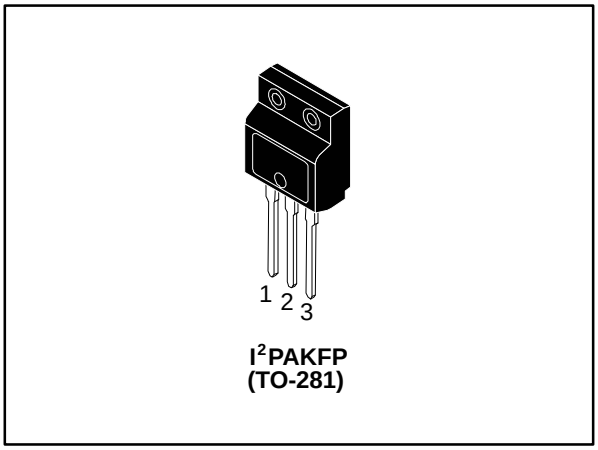
STFI15N95K5

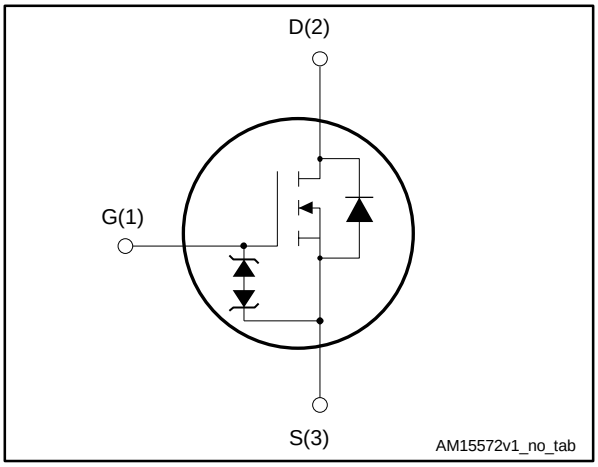
N-channel 950 V, 0.41 Ω typ., 12 A MDmesh™ K5 Power MOSFET in a I²PAKFP package

Datasheet - production data



I²PAKFP (TO-281)

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{tot}
STFI15N95K5	950 V	0.50 Ω	12 A	30 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STFI15N95K5	15N95K5	I²PAKFP (TO-281)	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	7.6	A
I_{DM} (2)	Drain current pulsed	48	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
ESD	Gate-source human body model (R= 1,5 kΩ, C = 100 pF)	2	kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	2500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 12 A, di/dt ≤ 100 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$

(4)V_{DS} ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	124	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	950			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 950 V, V_{GS} = 0 V			1	µA
		V_{DS} = 950 V, V_{GS} = 0 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ± 20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.41	0.50	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	855	-	pF
C_{oss}	Output capacitance		-	65	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 760 V	-	104	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related			38	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 12 A V_{GS}= 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	30	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	22	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 475 V, I_D = 6 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 15: "Test circuit for resistive load switching times"* and *Figure 18: "Unclamped inductive load test circuit"*)	-	23	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	62	-	ns
t_f	Fall time		-	11	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}	Source-drain current (pulsed)		-		48	A
V_{SD}(1)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	444		ns
Q_{rr}	Reverse recovery charge		-	7		µC
I_{RRM}	Reverse recovery current		-	32		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	630		ns
Q_{rr}	Reverse recovery charge		-	9.2		µC
I_{RRM}	Reverse recovery current		-	29		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

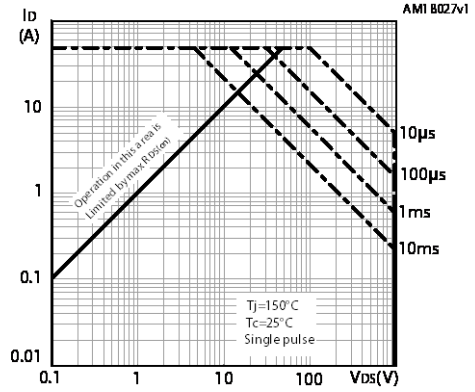


Figure 3: Thermal Impedance

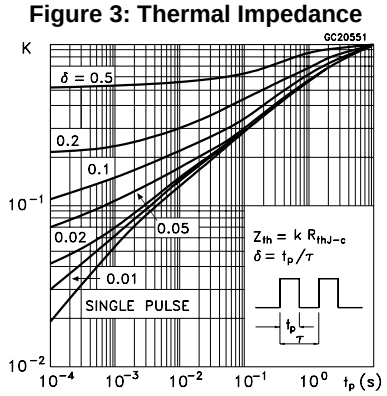


Figure 4: Output characteristics

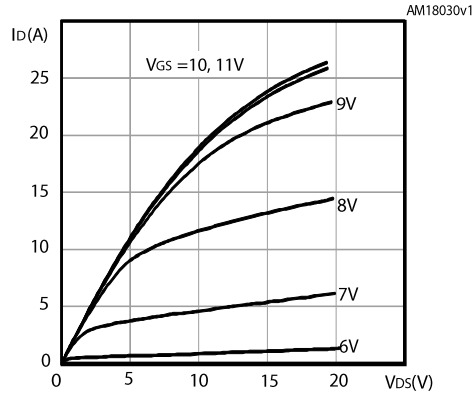


Figure 5: Transfer characteristics

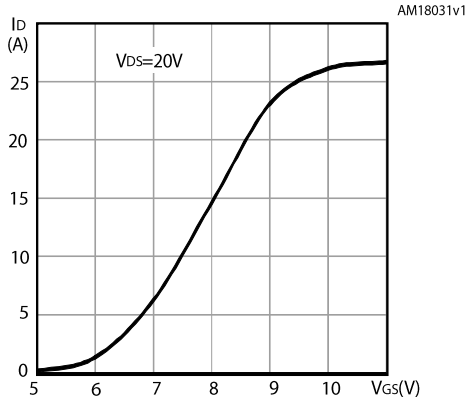


Figure 6: Gate charge vs gate-source voltage

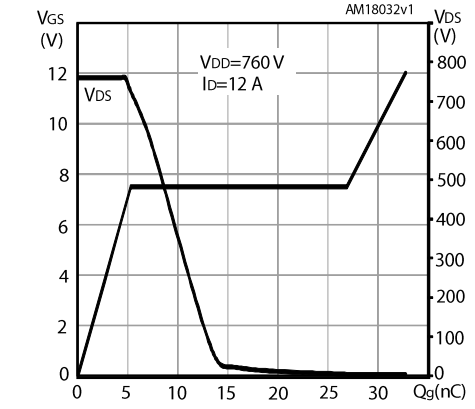


Figure 7: Static drain-source on-resistance

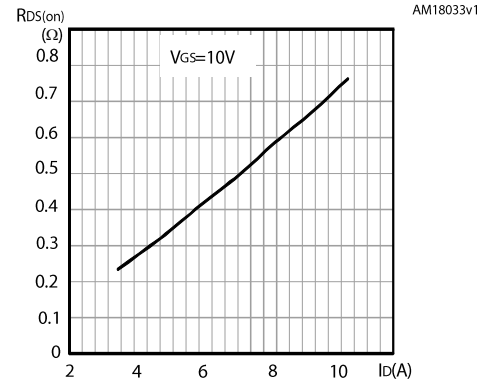


Figure 8: Capacitance variations

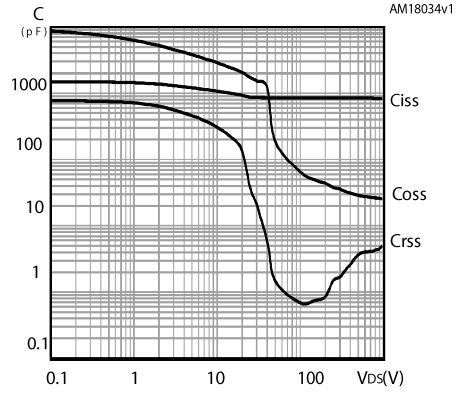


Figure 9: Output capacitance stored energy

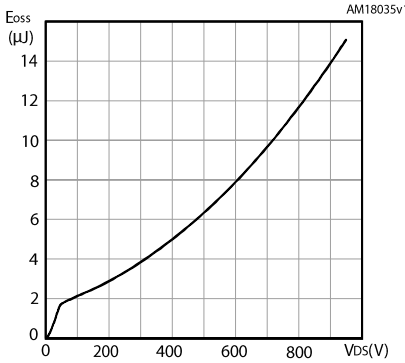


Figure 10: Normalized gate threshold voltage vs temperature

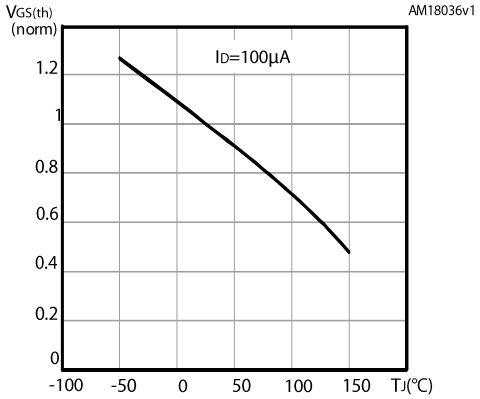


Figure 11: Normalized V(BR)DSS vs temperature

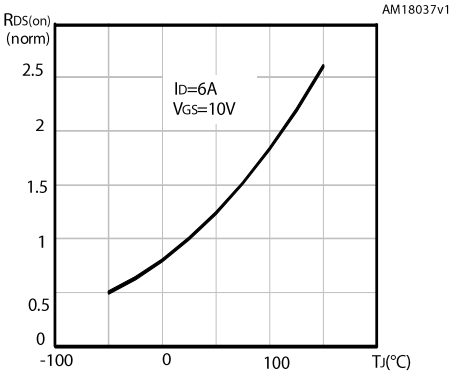


Figure 12: Normalized VDS vs temperature

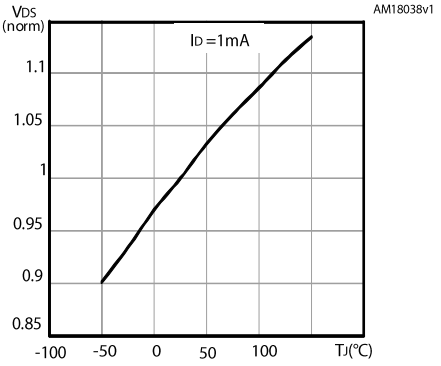


Figure 13: Source-drain diode forward characteristics

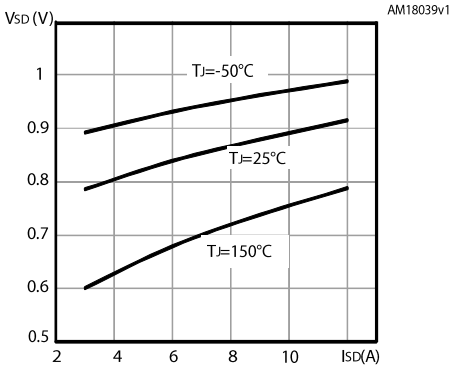
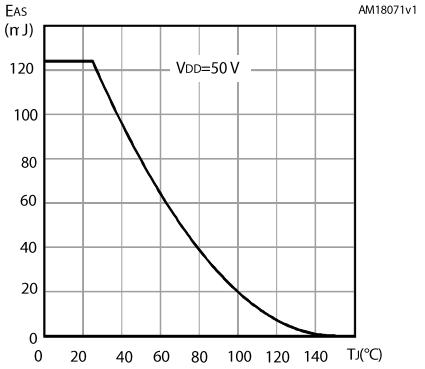


Figure 14: Maximum avalanche energy vs starting TJ



3 Test circuits

Figure 15: Test circuit for resistive load switching times

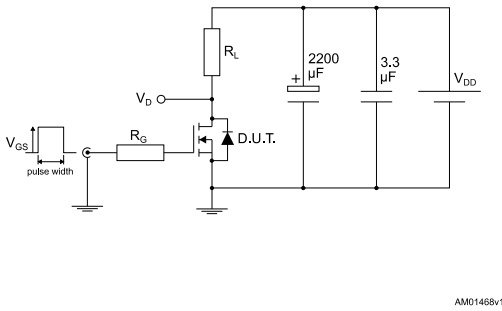


Figure 16: Test circuit for gate charge behavior

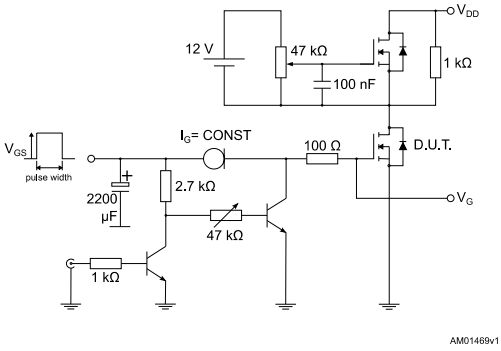


Figure 17: Test circuit for inductive load switching and diode recovery times

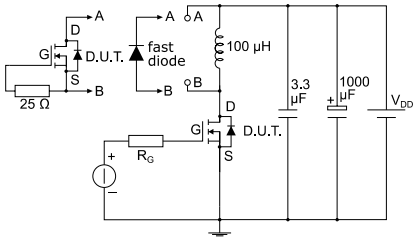


Figure 18: Unclamped inductive load test circuit

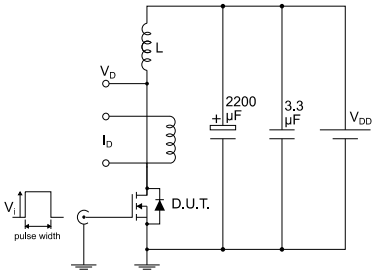


Figure 19: Unclamped inductive waveform

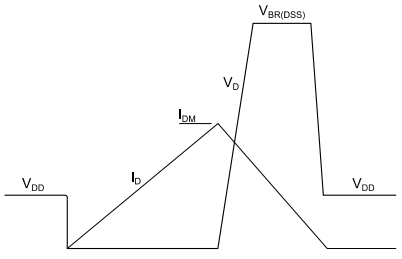
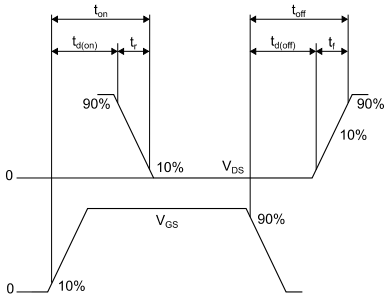


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 I2PAKFP (TO-281) package information

Figure 21: I²PAKFP (TO-281) package outline

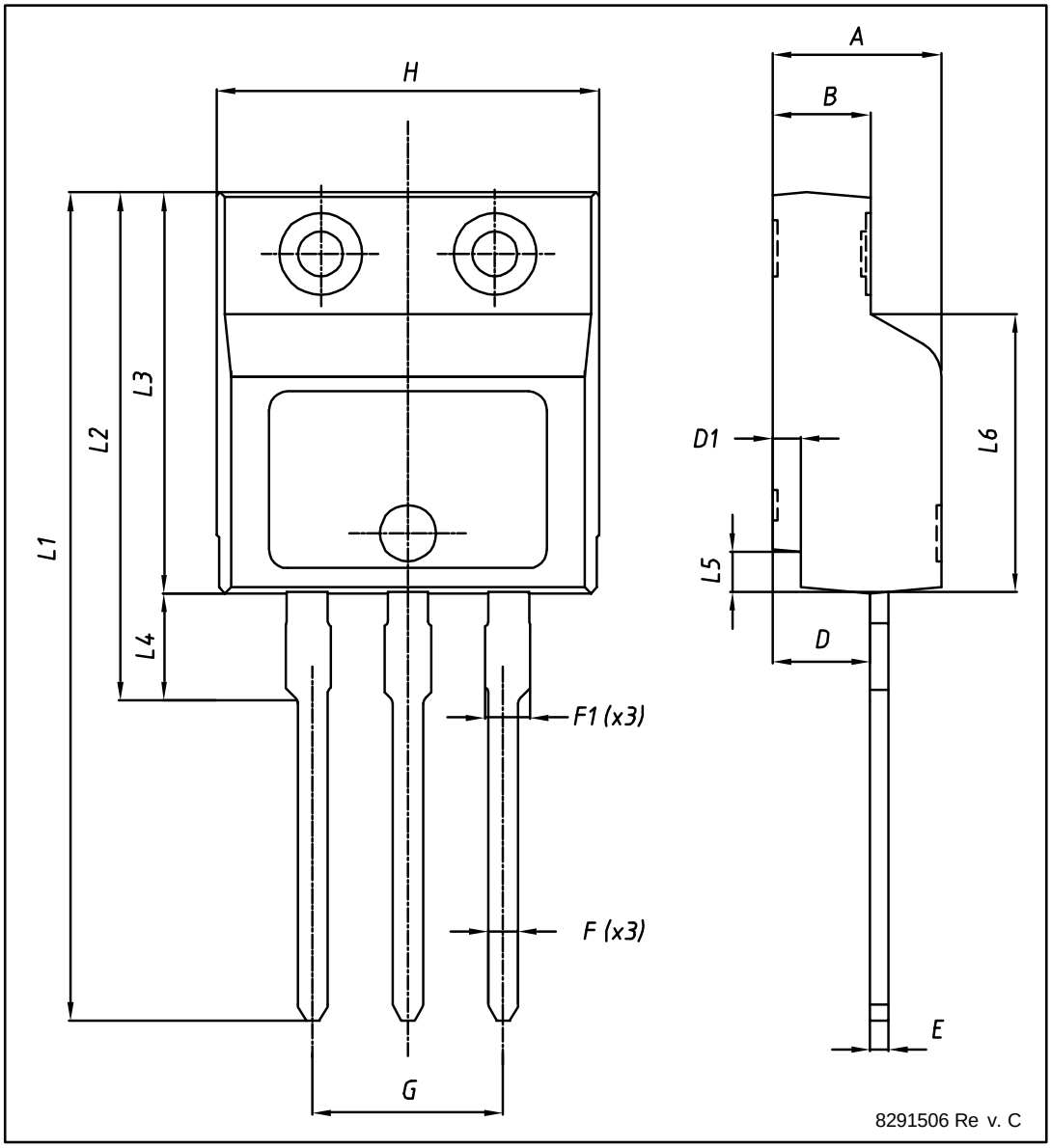


Table 10: I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
29-Jul-2016	1	First release.

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